SYMPOSIUM T

Structure and Electronic Properties of Ultrathin Dielectric Films on Silicon and Related Structures

November 29 – December 1, 1999

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* Invited paper

SESSION T1:
Monday Morning, November 29, 1999
Room 310 (H)

8:30 AM *T1.1
DYNAMICS OF SILICON OXIDATION. A.M. Stoneham, Dept of Physics and Astronomy, University College London, London, UK.

The rate-determining process in dry oxidation of silicon for thicker oxides (say above 10 nm) is probably the interstitial diffusion of oxygen molecules. For the thinner oxides (a few nm), this simple picture is inadequate. The Deal-Grove model of oxidation kinetics fails. Oxide usually grows by a layer-by-layer process (so far as is possible for an amorphous oxide), but with growth at terraces, not steps. The oxide shows oscillatory roughening. Isotope experiments show that exchange of interstitial and network oxygens occurs close to the Si/oxide interface and close to the oxide/gas interface. These observations point to limiting mechanisms other than diffusion, and mainly to processes involving charged oxygen species. It is important that, since silicon is significantly more polarisable than the oxide, there is an image interaction which biases adsorption and incorporation of oxygen species to those sites which correspond to thinner oxide. We have made parameter-free LDA calculations for a range of neutral and charged oxygen species to assess relative stabilities, diffusion mechanisms, and tendency to isotope exchange. These results have implications for acceptable mechanisms. We have also used Monte-Carlo methods to examine the consequences of the image interaction bias, and we have initial models of the charge transfer processes which lead to the formation of charged species. I shall also comment on the implications for oxide quality, and especially on the quality and the relationship between charge and energy localisation processes.

9:00 AM T1.2
TIGHT-BINDING MOLECULAR DYNAMICS SIMULATION OF SILICON PLASMA OXIDATION. Aruba Yamada, Seiichi Tamami, Akira Endou, Momoji Kubo, Akira Miyamoto, Tohoku Univ., Dept. of Materials Chemistry, Sendai, JAPAN; Akiko N. Itakura and Masahiro Kitajima, National Research Institute for Metals, Tsukuba, JAPAN.

According to the recently fabricated silicon device technology, the thickness of gate oxide is only a few nanometers. Hence, the effect of device characteristics resulted from the flatness of SiO_2/Si interface and the bonding state of the transition region can not be neglected. Plasma oxidation [1] is a technique being used for growing insulator films on semiconductor surfaces at lower temperature than that used for thermal oxidation. In this study, we performed the plasma oxidation simulation using the tight-binding molecular dynamics, the oxygen species are emitted over the substrate and the structure of constracted SiO_2 film was discussed. The TBMD calculations were performed by Colors [2] code developed by our group. The parameter used in the TB Hamiltonian are determined by a fit of the tight-binding results to the binding energy, bond length and frequencies of the density functional calculations. We used the cluster model representing H-Si(100)2×1 surface. Ten oxygen atoms were emitted from the initial position located above the surface by 10 Å at intervals of 0.2 ps. The total time in present TBMD calculations was 2.46 ps. In order to discuss energy dependence of our results, we choose the initial kinetic energy of oxygen atoms to be 4, 8, 12 and 16eV. We calculated the in-depth profile of oxygen atoms at various bombardment energies, and we can confirm that the surface is oxidized intensively when the bombardment energy is low and the deeper layers are oxidized when the energy is higher than 10eV. [1] M. Kitajima, I. Kamioka, K.G. Nakamura and S. Hishita, Phys. Rev. B 53, (1996) 3993. [2] A. Yamada, A. Endou, H. Takaba, K. Teraishi, S.S.C. Ammal, M. Kubo, K.G. Nakamura, M. Kitajima and A. Miyamoto, Jpn. J. Appl. Phys. 38, (1999) 2434.

9:15 AM T1.3
UNIVERSAL THEORY OF OXIDE GROWTH RATE ON SILICON. Hiroyuki Kageshima, Kenji Shiraishi, NTT Basic Research Labs, Kanagawa, JAPAN.

Silicon-atom emission from interfaces in silicon oxidation is known as the source of the selfinterstitials in OSF (Oxidation-induced Stacking Faults). At the last two fall meetings, we reported on newly found atomic-scale views for the mechanism of the silicon-atom emission by using the first-principles calculation method. In this study, we theoretically point out the essential role that emitted silicon atoms play in determining the silicon-oxide growth rate. First, we evaluate the silicon-atom emission rate during oxidation by using the first-principles calculation method. The results show that at least one silicon atom is emitted from the interface during the oxidation of eight silicon atoms. Since such a large amount of the emitted silicon atoms should govern the oxide reaction rate at the interface, we have developed a new theory for the oxide growth rate taking account the silicon-atom emission rate. Our constructed equation of the oxide growth rate is identical to that of the widely accepted Deal-Grove theory when the oxide is thick. In addition, when the oxide is thin, our equation reproduces the empirical equation for the initial enhanced growth proposed by Massoud, et al. Consequently, with our theory, the oxide growth rate for the whole range of the oxide thickness can be explained without any empirical modifications, while the rate for an oxide thickness of less than 10 nm in dry oxidation cannot be explained with the Deal-Grove theory. Thus, we have succeeded in constructing a new non-empirical universal theory of the silicon oxide growth rate based on the first-principles calculations. Furthermore, our theory is also applicable for discussing the nitridation, the oxynitridation of the silicon, and the dielectric reliability of the formed oxide (oxynitride) layers.

9:30 AM T1.4
ATOMIC AND ELECTRONIC STRUCTURE OF SEMICONDUCTOR/OXIDE INTERFACES. Gerd Duscher, Ryszard Buczko, Stephen J. Pennycook and Sokrates T. Pantelides, Vanderbilt University, Department of Physics & Astronomy, Nashville, TN; Oak Ridge National Laboratory, Solid State Division, Oak Ridge, TN.

We use the combination of atom column resolved Z-contrast imaging and electron energy-loss spectroscopy (EELS) to study a variety of interfaces between silicon dioxide and semiconductors. A comparison to theoretical calculations (R. Buczko et al.: this symposium) allows one to determine the oxide structures present at the (100) Si/SiO_2 interface. Both silicon substrates with (111) and (100) surface orientation and 4H-SiC substrates were thermally oxidized in dry or wet ambients.
To determine the structure of the crystalline phase of this interface, we use Z-contrast imaging in a 300kV dedicated STEM (VG HB603 U) with a point resolution (FWHM of beam diameter) better than 0.13 nm. With this atom column resolved Z-contrast imaging, we determined directly the atomic structure of the substrate at the interface. All the samples had an interface roughness of one atomic layer. This is surprisingly smooth for the SiC/SiO interface, although, at this interface, large accumulated steps due to the misscut are present. The images showed no evidence for crystalline oxide.
The same samples were also studied with EELS at a 100 kV dedicated STEM (VG HB501 UX) with an optimum beam diameter (FWHM) of 0.22 nm. EELS is not only used to study the chemical composition but the electron-loss near edge structure (ELNES) of the ionization edge is (in a first approximation) the local momentum projected density of states of the conduction bands. An analysis of the ELNES of the Si–$L_{2,3}$ and O–K revealed the presence of silicon rich oxide, the basic structure most likely in the form of quartz or cristobalite at the (100) Si–interface. This does not coincide with the equilibrium structure calculated by density functional theory, indicating that there is still room for improvement of this important interface.

10:15 AM *T1.5
CHARACTERISATION OF THE P_{b1} INTERFACE DEFECT IN THERMAL (100)Si/SiO_2 BY ESR: ^{29}Si HYPERFINE STRUCTURE AND ELECTRICAL RELEVANCE. Andre Stesmans, Department of Physics, University of Leuven, Leuven, BELGIUM.

The P_b-type centers are electron spin resonance (ESR) active point defects inherently incorporated at the thermal Si/SiO_2 interface as a result of mismatch, with at least one variant operating as a detrimental charge trap. Their appearance depends on the crystallographic interface orientation: the (111) and (100) interfaces exhibit the P_b and P_{bo}, P_{b1} centers, respectively. While P_b and P_{bo} appear similar, P_{b1}, the archetype defect for the (100)Si/SiO_2 interface, has so far eluded atomic identification. Here, we report on enhanced ESR experiments that have succeeded in resolving the full angular dependence of ^{29}Si hyperfine interaction. As a major result, the data uncover the defect as a prototype Si dangling bond defect with, however, the unpaired sp^3 Si orbital approximately oriented along a <211> direction at ~35° with the [100] interface normal. The incorporation of this defect kernal into a larger defect structure will be discussed in connection with theoretical insight. Additionally, the electrical aspects of P_{b1} in connection with its behavior under thermal load have been investigated, the latter including postoxidation annealing in various ambients. These data together with enhanced ESR monitoring enable faithful assessment of the defect's electrical impact. The results will be overviewed in the light of trying to better understand the defects archetypical appearance at the (100)Si/SiO_2 interface.

10:45 AM *T1.6
IN-SITU ESR OBSERVATION OF OXIDATION PROCESS OF SILICON. Satoshi Yamasaki, Takahide Umeda, Ujjwal K. Das, Masayasu Nishizawa, Tetsuji Yasuda and Junichi Isoya, Joint Research Center for Atom Technology (JRCAT), Tsukuba, JAPAN.

We have developed in-situ ESR to observe the initial stages of oxidation of crystalline Si. An UHV chamber with a base pressure

below 10^{-10} Torr was placed inside the ESR cavity. Before oxidation, the Si surface were cleaned by direct current heating to 1100C. Transient ESR signals were observed after the introduction of oxygen gas at room temperature. For oxide films up to 1 monolayer thick, the new transient centers related to the Pb center appeared. When the oxide grew thicker, the transient centers disappeared, and the generally observed P_b centers appeared. This ESR data is used to propose a microscopic model of the initial oxidation. In addition to the in-situ ESR study, detailed information about the defect centers for thicker films was derived by using pulsed ESR, combined with a low-temperature γ-ray irradiation

11:15 AM T1.7
DETECTION OF INTERFACE STATES CORRELATED WITH LAYER-BY-LAYER OXIDATION ON Si(100). Takeo Hattori, Hiroshi Nohira, Yukihiro Teramoto, Norikatsu Watanabe, Musashi Institute of Technology, Dept of Electrical & Electronic Engineering, Tokyo, JAPAN.

The root-mean-square(rms) surface roughness exhibits oscillation with a period in the oxide film thickness of 0.19 nm up to the thickness of 2 nm. The amplitude of this oscillation does not change from 0.5 to 2 nm. Based on the observation of surface morphology and the measurement of interface structure, this oscillation was attributed to the layer-by-layer oxidation reaction at the interface over the area of 5 nm $\times$ 5 nm.[1] In accordance with this oscillation, the interface-state (IS) distribution in Si bandgap exhibits periodic changes with progress of oxidation. Namely, IS density near the midgap of Si exhibits drastic decrease at the thickness where the roughness takes its minimum value, while that does not exhibit decrease at the thickness where the roughness takes its maximum value. Here, IS densities were measured non-destructively using the method developed by Lau et al.[2] The changes in electric potentials of surface and interface produced by applying voltage across the oxide film, which are necessary for the determination of IS densities, were measured as the shifts in C 1s core level of 2-propanol adsorbed on the oxide film and those in Si 2p core level of Si substrate induced by the electron-beam irradiation with electron kinetic energy of 2 eV. Therefore, the thickness should be precisely controlled with the accuracy of less than 0.1 nm in order to minimize the IS densities. [1] T. Hattori, M. Fujimura, and H. Nohira : MRS(Spring,1999)R3.1. [2] W. M. Lau and X. -W. Wu, Surf. Sci. **245**, 345 (1991).

11:30 AM T1.8
DEFECT STATES DUE TO SILICON DANGLING BONDS AT THE $Si(100)/SiO_2$ INTERFACE AND THE PASSIVATION BY HYDROGEN ATOMS. Chioko Kaneta, Takahiro Yamasaki, Fujitsu Laboratories Limited, Atsugi, JAPAN; Toshihiro Uchiyama, Tsuyoshi Uda, JRCAT-ATP, Tsukuba, JAPAN; Kiyoyuki Terakura, JRCAT-NAIR, Tsukuba, JAPAN.

The Si dangling-bonds (SDBs), the typical intrinsic defects at the Si/SiO_2 interface, have been considered to be one of the origins of the interface states, which is harmful to the performance and the reliability of MOS (metal-oxide-semiconductor) devices. In the $Si(100)/SiO_2$ interface, Pb0 and Pb1 centers have been known as SDB-type defects. We investigated the defect states due to the SDBs at the interface by employing the first-principles method based on the density functional theory. The generalized gradient correction and the spin polarization were taken into account. We considered two prototypes of SDB defects at the $Si(100)/SiO_2$ interface, SDB1 and SDB0. The SDB0 exists on one end of a Si-Si dimer and includes no O atoms. It has basically the same structure as the recently proposed model for the Pb1 center. On the other hand, the SDB1 exists on an edge of a Si-O-Si bridge and includes an O atom. The stable atomic configurations and the electronic structures for these systems were calculated to investigate the interface states. For the SDB0, two defect states appear in the band gap. This corresponds to the results obtained by DLTS measurements. We found that the states are strongly localized on the SDB at the interface. The lower state is occupied and the upper one is unoccupied in the neutral charge state. The SDB1 also generates two defect states. But the upper level is in the conduction band, while the lower level is in the band gap. We introduced a H atom into the interface to terminate the SDB1 and SDB0. The atomic configurations of the systems were optimized again. From the calculated electron densities of states, it was shown that the interface states completely disappear as a result of the introduction of the H atom.

11:45 AM T1.9
SURFACE AND INTERFACIAL TOPOGRAPHY OF OXIDES ON Si(111) WITH ULTRA-LOW ATOMIC STEP DENSITY. Antonio C. Oliver, Jack M. Blakely, Cornell University, Dept of Materials Science and Engineering, Ithaca, NY.

Atomic force microscopy has been used to study the morphology of oxide surfaces and $Si\text{-}SiO_2$ interfaces after oxidation of Si(111) surfaces that are either totally free of atomic steps or have well characterized low step density. The step-free areas were formed by thermally processing a patterned Si surface in which flat areas are enclosed by a square array of ridges.; flow of the atomic steps into the surrounding ridge barriers produces a regular array of step-free areas each of which can be up to $\sim$50x50 microns. Widely spaced (eg 5 micron) step arrays can also be produced in the step-free areas. AFM scans of the same areas were taken prior to (dry) oxidation, after oxidation, and after chemical removal of the oxides. It was found that at an oxide thickness in the 5-10nm range, the initial step structure of the underlying Si substrates is translated through the oxide to the surface after oxidation with the oxide surface being somewhat rougher than the initial substrate. Furthermore, the initial step arrangement of the substrate remains at the $Si\text{-}SiO_2$ interface after etching away the oxide by HF. The interface roughness is less than that of the oxide surface. Quantitative roughness measurements will be reported. The results suggest that the initial oxidation of silicon proceeds in a layer by layer manner and not through a preferential step-flow oxide growth mode. A process for further reduction of the roughness of the SiO_2 surface will be described.

SESSION T2:
Monday Afternoon, November 29, 1999
Room 310 (H)

1:30 PM *T2.1
XPS STUDIES OF THE Si/SiO_2 INTERFACE WITH SYNCHROTRON RADIATION. F. Rochet, F. Jolly, G. Dufour, University of Paris VI, FRANCE; C. Grupp, A. Taleb, F. Sirotti, LURE, Orsay, FRANCE.

Si 2p core-level spectroscopy is a unique tool to determine the chemical composition and spatial extension of the suboxide layer present at the Si/SiO_2 interface. In the case of ultra-thin oxide films (<10 $\AA$), the high surface sensitivity provided by the tunability of synchrotron radiation allows the observation of four energetically well-separated oxidation states, generally attributed to a silicon atom with an increasing number of oxygen first neighbors, and hence often denoted Si^{x+} (with x=1,..,4). First, we shall give an account of the heated debate concerning the possible contribution of the second oxygen neighbor shell to the chemical shift [1-2], which, if effective, would modify the picture of the interface. Second, we shall briefly discuss the quantitative issue [3]. Third, we shall examine the benefit derived from the use of very high energy resolution (better than 70 meV at $h\nu$=130 eV), and we shall try to determine, for this system, what are the limits of this spectroscopy. To illustrate the latter point, among various case studies (thermal oxides, adsorption at room temperature etc.) we shall treat in more detail the case of the H-terminated Si(111) surface oxidized by atomic oxygen, and discuss our data in the light of previous XPS [4] and vibrational spectroscopy [5] studies. References: [1] M. Banaszak Holl, S. Lee, F.R. McFeely, Phys. Rev. Lett. 72 (1993) 2441 [2] A. Pasquarello, M.S. Hybertsen, R. Car, Phys. Rev. Lett. 74 (1995) 1024 [3] F. Rochet, Ch. Poncey, G. Dufour, H. Roulet, C. Guillot, F. Sirotti, J. Non Cryst. Solids, 216 (1997) 148 [4] H. Ogawa and T. Hattori, Appl. Phys. Lett. 61 (1992) 577 [5] H. Ikeda, Y. Nakagawa, M. Toshima, S. Furuta, S. Zaima, Y. Yasuda, Appl. Surf. Sci. 117/118 (1997) 109

2:00 PM T2.2
A NEW STRUCTURAL MODEL FOR SILICON/SILICON-OXIDE INTERFACES DERIVED FROM SILOXANE CLUSTERS: IMPLICATIONS FOR PHOTOEMISSION SPECTROSCOPY. Krishnan Raghavachari, Joseph Eng, Jr., Bell Laboratories, Lucent Technologies, Murray Hill, NJ.

The interpretation of Si 2p photoemission spectra of the silicon/ silicon oxide interface has been controversial. The conventional first nearest neighbor model (i.e., based on the formal oxidation state of Si) has been questioned based on the photoemission spectra of interfaces derived from the interaction of spherosiloxane and related clusters with the Si(100) surface. In this work, we perform a detailed theoretical investigation of the reaction of such clusters with Si(100) using gradient-corrected density functional methods, and resolve this controversy. Using transition state studies of competing reaction pathways, we propose a new structural model for the resulting silicon/silicon oxide interface. The implications of our results for the interpretation of core-level photoemission spectra will be discussed.

2:15 PM T2.3
QUANTITATIVE MEASUREMENTS ON ROUGHNESS AT Si/SiO_2 INTERFACES AND THEIR IMPLICATIONS. Xidong Chen, J M. Gibson, Materials Science Division, Argonne National Laboratory, Argonne, IL.

With a plan-view transmission electron microscopy technique to directly image buried Si/SiO_2 interfaces, we studied the interface

roughness resulting from the oxidation process. We first obtained direct experimental evidence that the height-height auto-correlation function is a Gaussian function at Si(111)/SiO_2 interfaces. This Gaussian auto-correlation function is a natural consequence of step motion during silicon oxidation according to a kinetic model that we developed. Xidong Chen and J. M. Gibson, Phys. Rev. Lett. 81, 4919 (1998). Our results indicate that roughness may provide insights on oxidation kinetics. Si(100)/SiO_2 interfaces are however more complicated. Our previous studies showed that thermal annealing at 900°C dramatically removed roughness. In this talk, we will provide detailed quantitative measurements on Si(100)/SiO_2 interface roughness. The experimental results will be compared with our modeling.

2:30 PM T2.4
PRECISE CHARACTERIZATION OF ULTRATHIN OXIDE/ NITRIDE/OXIDE STRUCTURES BY GRAZING X-RAY REFLECTANCE AND SPECTROSCOPIC ELLIPSOMETRY IN THE UV AND NEAR INFRARED RANGE. Pierre Boher, Jean Philippe Piel and Jean Louis Stehle, SOPRA SA, Bois Colombes, FRANCE.

Precise characterization of ultrathin oxide/nitride/oxide (ONO) structures becomes a challenging task due to the very low thickness (<3-4nm), which will be needed in the next generation of gate dielectrics. Conventional techniques such as spectroscopic ellipsometry in the visible range becomes difficult to apply because of the great correlation between thickness and optical indices. To overcome this problem one solution is to extend the wavelength range in the deep UV range (down to 157nm) where the nitride becomes very absorbant or in the near IR range (up to 18μm) where the Si-N and Si-O dangling bounds can be discriminated. This kind of analysis has been made on a serie of ONO samples with variable thickness and degree of nitridation. Regression results obtained in the different wavelength ranges will be compared and discussed. Results will be also compared to grazing x-ray reflectance measurements made on the same samples with the combined SOPRA grazing x-ray reflectometer/ spectroscopic ellipsometer system. Results will be also compared to those obtained by other authors using TEM, SIMS and XPS on the same samples, and the advantages of the different techniques will be discussed.

2:45 PM T2.5
INFLUENCE OF PRE AND POST PROCESS CONDITIONS ON THE COMPOSITION OF THIN Si_3N_4 THIN FILMS (3 NM) STUDIED BY XPS AND TOFSIMS. T. Conard, H. De Witte, W. Vandervorst, M. Houssa, M. Heyns, IMEC, Leuven Belgium; C. Pomarede, C. Werkhoven, ASM America, Phoenix, AZ.

With the downscaling of the electronic devices and the increase in the frequency of the electronic circuits, a large search for new gate dielectric is ongoing. The exact composition and element distribution in the dielectric film have a large impact on the electrical characteristics of these films. We studied here the formation of ultrathin Si_3N_4 films (~3 nm) under different conditions and concentrated on their composition analysis. The Si substrates were cleaned using NCC and/or HF dip. The Si_3N_4 films were subsequently fabricated either by RTCVD (SiH_4/NH_3) either by remote plasma (SiH_4/N_2) with or without a pre-anneal to form a 0.5 nm SiO_2 layer. Post annealing was made using NO, NO_2 or NH_3 at various temperatures and for various times. The quantification of the composition was realized using XPS and elemental distribution was analyzed using TOFSIMS with Ar^+ sputtering and positive ion detection mode. The results show that the fabrication method of the nitride film has only a very limited influence on the O/N content of the films. However, both the preparations of the substrate (HF last or NCC last) and the post-annealing influence strongly the film composition. The presence of an interfacial oxide increases significantly the oxygen content of the film. Post-annealing with NO_2 also increases the oxygen content of the film while the NH_3 post-annealing leads to a significant decrease. The results will be compared with electrical characterization of the same films.

3:30 PM *T2.6
THE END OF THE ROADMAP FOR SILICON DIOXIDE: THE ELECTRONIC STRUCTURE OF HYPER-THIN GATE OXIDES AT THE ATOMIC SCALE. D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt and G. Timp, Bell Labs, Lucent Technologies, Murray Hill, NJ; J. Neaton, Physics Dept, Cornell University, Ithaca, NY.

The narrowest feature on an integrated circuit is currently the gate oxide. In less than 10 years, the semiconductor industry roadmap calls for gate oxides having a capacitance equivalent to that of 1 nm of silicon dioxide. If silicon dioxide is still to be used, then the projected gate oxide thickness will be less than 5 silicon atoms across. At least two of those five atoms will be at the silicon/oxide interfaces. The interfacial atoms have very different electrical and optical properties from the desired bulk silicon dioxide yet comprise a significant fraction of the dielectric layer. Using atomic-scale energy loss spectroscopy (EELS) in a scanning transmission electron microscope (STEM), we have imaged the chemistry and electronic structure profiles of gate oxides between 3 and 30 silicon atoms thick. We are able to resolve the interfacial states resulting from the spillover of the silicon conduction band wavefunctions into the oxide. The spatial extent of these states places a fundamental limit on the thinnest usable silicon-dioxide gate dielectric of 0.7 nm (4 silicon atoms across). Interface roughness increases the minimum usable thickness for present growth techniques. The effects on the leakage and drive currents from 35-60 nm transistors manufactured using these oxides will be discussed.

4:00 PM T2.7
DEPOSITION AND CHARACTERIZATION OF ULTRA-THIN Ta_2O_5 LAYERS DEPOSITED ON SILICON FROM A $Ta(OC_2H_5)_5$ PRECURSOR. Christophe Chaneliere, Jean-Luc Autran, LPM, INSA Lyon, Villeurbanne, FRANCE; Jean-Philippe Reynard, Jean Michailos, Kathy Barla, STMicroelectronics, Crolles, FRANCE; Akihiko Hiroe, Kouji Shimomura, Akinobu Kakimoto, TEL, Yamanashi, JAPAN.

The scaling-down of silicon integrated circuits has led to the emergence of high permittivity materials to propose an alternative to the insulators commonly employed in microelectronics, i.e., SiO_2 and Si_3N_4. Due to its high dielectric constant (~25 for the amorphous phase) and its low leakage currents through thin layers as compared to other high permittivity insulators (such as TiO_2, (Ba,Sr)TiO_3 or Pb(Zr,Ti)O_3), tantalum pentoxide (Ta_2O_5) appears to have been adopted for use as a dielectric layer for storage capacitors of DRAMs, and is also foreseen for applications such as the gate dielectric of MOSFETs or the insulating layer of integrated MIM capacitors. Ta_2O_5 films can be deposited by the conventional CVD methods. Nevertheless, the properties of Ta_2O_5 layers must be improved, and the study of the influence of the interfacial SiO_2 layer (practically inevitably grown between Ta_2O_5 and Si during deposition and post-deposition annealing) or the interfacial Si_3N_4 film (formed before Ta_2O_5 deposition to limit or avoid the oxidation of the substrate) on the electrical properties of Ta_2O_5-based capacitors is necessary to improve these properties. In this work, amorphous Ta_2O_5 layers were deposited on 8-inch. Si(100) substrates by LPCVD from a $Ta(OC_2H_5)_5$ precursor with three targeted thicknesses: 6, 8 and 10 nm (respectively equivalent to ~1, 1.3 and 1.6 nm of SiO_2). Prior to deposition, the silicon substrates were submitted to a rapid thermal nitridation (RTN) treatment. Post-deposition annealings were then performed in UV-O_3, O_2 or a combination of these two treatments. In the final paper, we will report the detailed characterization of the Ta_2O_5/Si interfacial region by high resolution TEM and SIMS analysis as well as the electrical properties of Ta_2O_5-based MOS capacitors issued from the same wafers. Results concerning leakage current densities, global dielectric constant and oxide and interface trapped charges will be reported.

4:15 PM T2.8
HIGHLY RELIABLE THIN HAFNIUM OXIDE GATE DIELECTRIC. Laegu Kang, Byounghun Lee, Wen-Jie Qi, Yongjoo Jeon, Renee Nieh, Sundar Gopalan, Katsunori Onishi, and Jack C. Lee, University of Texas and Microelectronics Research Center, University of Texas at Austin, Austin, TX.

Hafnium oxide (HfO_2) is one of the possible gate dielectrics for sub 0.1μm regime because of its high K and thermal stability on silicon. In this study, ultra thin (EOT ~ 1.6nm) MOS capacitor with HfO_2 gate dielectric and Pt electrode was fabricated. HfO_2 was deposited using reactive sputtering of Hf target in an O_2+Ar ambient. The area of the capacitor is $5x10^{-5}cm^2$. Leakage currents of 1.6nm HfO_2 films are about $1x10^{-4}/cm^2$ at +1.0V with breakdown field of ~8MV/cm. The leakage current are three orders of magnitude lower than that of SiO_2 film. The refractive index, n is ~2.1 and the dielectric constant for MIM structure with HfO_2 dielectric was 25~28. From the XPS data, HfO_2 became more stoichiometric as the post Pt annealing temperature increased. Detailed processes and characteristics (e.g. hysteresis and frequency dispersion) will be also presented.

4:30 PM T2.9
DEPOSITION OF ZrO_2/SiO_2 FILMS BY REMOTE PLASMA-ASSISTED CHEMICAL VAPOR DEPOSITION FOR GATE DIELECTRICS IN AGGRESSIVELY SCALED CMOS DEVICES. Robert Therrien, G. Bruce Rayner, Gerald Lucovsky, North Carolina State University, Dept of Physics, Raleigh, NC.

The need for aggressively-scaled CMOS devices to meet ULSI performance requirements has created the need for alternative gate dielectric materials to replace SiO_2. It is necessary that the alternative dielectric material have a dielectric constant that is higher than that of SiO_2 so physically-thicker films will be equivalent to thinner oxides with reduced direct tunneling current. To this end zirconium silicate

($ZrSi_xO_y$) films have been deposited by remote plasma-assisted chemical vapor deposition at 300°C using O-species extracted from an upstream O_2/He plasma, downstream injected Zr(IV) t-butoxide and silane as the precursor materials. FTIR, TEM and electron diffraction have demonstrated that these films are amorphous as-deposited and remain amorphous upon annealing up to 900°C in an inert ambient. Compositional analysis of the deposited films has been performed using on-line AES, FTIR, and RBS techniques. For example the AES demonstrated (1) Zr and Si are bonded to O and (2) no evidence of Zr-Si bonding. This paper identifies the process in which the relative concentrations of ZrO_2 to SiO_2 have been controlled to achieve specific compositions. Properties of these films that are relevant to their role as an alternative dielectric material, such as capacitance-voltage, current-voltage and optical band-gap, are also discussed. Supported by NSF, SEMATECH, and ONR.

4:45 PM T2.10
BAND LINE-UPS OF HIGH K DIELECTRICS BST, Ta_2O_5, $BaZrO_3$, Al_2O_3 AND Y_2O_3 ON Si AND Pt. J. Robertson, E. Riassi, Engineering Department, Cambridge University, UK, J-P. Maria, A.I. Kingon, Dept of Materials Science and Engineering, North Carolina State University, Raleigh, NC.

High dielectric constant materials such as Ta_2O_5 and Barium strontium titanate (BST) are needed for DRAM capacitor and gate dielectrics in future silicon devices. The band offsets of these new materials must be over about 1 eV for both electrons and holes in order to minimise leakage currents due to Schottky emission. We have calculated the band line-ups of many high K materials on Si and metals using the method of charge neutrality levels. We previously found that Ta_2O_5 and BST had rather small conduction band offsets on Si, because their band line-ups are quite asymmetric. Here, we extend the analysis to other possible wide gap materials. The zirconates such as $BaZrO_3$ and ZrO_2 have wider gaps than the titanates, but they still have rather low conduction band offsets on Si. On the other hand Al_2O_3 with a 8.8 eV gap and Y_2O_3 are found to each have offsets of over 1.5 eV for both electrons and holes, suggesting that these are preferable dielectrics. The implications of these results for future generations of MOSFETs and DRAMs are discussed.

SESSION T3: POSTER SESSION
Monday Evening, November 29, 1999
8:00 P.M.
Exhibition Hall D (H)

T3.1
DOUBLE LENGTH-SCALE ORDERED NANOPOROUS STRUCTURES OF SILICA FOR LOW-LOSS DIELECTRICS. J.S. Yin and Z.L. Wang, School of Materials Science and Engineering, Georgia Institute of Technology, Atlanta, GA.

Preparation of ordered nanoporous materials has vitally practical interests in catalysis and phonotics. In this paper, a three-dimensional ordered nanoporous structure of silica at double length-scales have been prepared for the first time with the template assistance of polystyrene spheres. The first length-scale is in the order of the polystyrene spheres of mean size ~ 200 nm, which are packed into a face-centered cubic (fcc) or hexagonal-close-packed (hcp) lattice and extend to macroscopic sizes. The second length-scale order is formed by infiltrating the fcc/hcp assembly with surfactants, leading to nanopores of ~ 10 nm in diameter. The composites was treated in a furnace at 450°C for 6 hours to burn out the polystyrene and the co-polymer surfactant, while the porous structures in the two length-scales were preserved. Scanning electron microscopy and transmission electron microscopy have shown the ordered structures. A comparison is given on the low-loss EELS spectra recorded from solid silica spheres, mesoporous silica and double-length scale ordered porous silica. The plasmon energy of the porous silica structures shows a significant shift in comparison to that of the bulk, suggesting that the local density of the bound electrons in the porous structures is likely to be lower than that in the bulk. Therefore, the imaginary part of the dielectric function also drops, leading to even lower dielectric loss in addition to that induced by the volume porosity. With consideration the flexibility of tunable porosity of the silica by changing the sizes of the template PS spheres and the chain length of the co-polymer, this study provides a technique for tuning the electronic structure of silica by varying its porosity. The porous materials are expected to have not only large surface area for catalysis, but also low dielectric constant for high-frequency microelectronics. [1] J.S. Yin and Z.L. Wang, Appl. Phys. Letts. 74 (1999) 2629. [2] Research sponsored by US NSF grant DMR-9733160, and the Outstanding Oversea Young Scientist Award of China NSF (59825503).

T3.2
MESOSCOPIC TRANSPORT IN BROKEN DOWN ULTRATHIN SiO_2 FILMS. Enrique Miranda, Jordi Sune, Rosana Rodriguez, Montserrat Nafria, Xavier Aymerich, Universitat Autnoma de Barcelona, Dept of Electronics Engineering, Barcelona, SPAIN.

It is well-known that the breakdown of ultrathin oxides consists in the formation of a highly localized low-resistance conduction path running between the electrodes. Two breakdown modes have been identified in such oxides which are referred to as soft (SBD) and hard (HBD) breakdown, in clear connection with the magnitude of the event. Although much effort has been devoted to understand the SBD mode, little emphasis has been put on its link with the HBD mode. We present a new analytic model based on the physics of mesoscopic conductors which covers both failure modes in a consistent way. Briefly, the electron motion becomes quantized in the transverse directions when passing through a narrow constriction. Depending on the electron energy, such discrete states can act as transmitting or backscattering conduction channels. A decomposition of the Schrodinger equation in tranverse and longitudinal equations permits to analyze the 3D problem as a 1D problem. As in a quantum well, the energy of the transverse discrete levels depend on the inverse of the constriction's cross-sectional area. Thus, the bottleneck of the constriction plays the essential role in the conducting behavior. Considering the transmission properties of an inverted parabolic barrier, we demonstrate that when the electron energy is above the top of the barrier, the conductance of the system corresponds to that observed experimentally for the HBD mode. This regime is associated with quantum point contact conduction. On the other hand, if the electron energy is well below the first subband level, the analytic expression for the current fits the SBD experimental data. The model also explains the independence of the breakdown I-V characteristic on the oxide thickness and gate area (only the geometrical features at the bottleneck of the constriction are relevant) as well as the link between slope and current level (lower slopes at larger currents for a fixed bias point).

T3.3
ROLES OF HOLE AND FN ELECTRON FLUENCES IN GATE OXIDE BREAKDOWN. M.F. Li, Y.D. He, S.G. Ma, Byung-Jin Cho, K.F. Lo,[1] and M.Z. Xu[2] CICFAR, Dept of Electrical Engineering, National University of Singapore, SINGAPORE, [1]Chartered Semiconductors Manufacturing Pte. Ltd, SINGAPORE, [2]Institute of Microelectronics, Peking University, Beijing, CHINA.

A simple model which links the hole and FN electron injections to oxide breakdown is established. This is of vital importance in predicting the lifetime of realistic CMOS device operation. pMOSFET in n well structure is used with a switching forward bias V_{inj} applying to the substrate to well junction with a switch-on duty cycle DUC. When V_{inj} switch-off, the gate current is mainly the FN tunneling current J_n . When V_{inj} switch-on, there is gate current increment $\Delta J = J_p{}^{pri} + \Delta J_n$, here $J_p{}^{pri}$ is the hole injection current from the substrate with hole fluence ${}_p{}^{pri}$, ΔJ_n is the increase of FN electron current, due to hole trapping in the oxide and thereby change the oxide field. We define trap densities $D^{pri} = \iota^{pri} Q_p{}^{pri}$ and $D_n = \iota^n Q_n$, where Q_n is electron fluence and ι is the probability of trap activation by each hole (or FN electron) per unit length . In our model, D^{pri} and D^n belong to same kind of traps and when the sum of D^{pri} and D^n reaches a critical value D_{cri}, the oxide breaks. Therefore, $Q_p{}^{pri} + (\iota^n/\iota^{pri}) * Q_n = D_{cri}/\iota^{pri} = Q_p{}^{pri}{}_{cri}$ (1) Running N times breakdown experiments by applying same stress condition but different DUC, we obtain N pairs of $Q_p{}^{pri}$ and Q_n with different $Q_p{}^{pri}/Q_n$ ratio. When N is very large, the experimental data show that $Q_p{}^{pri}$ correlates linearly with Q_n as predicted by (1). The constant $Q_p{}^{pri}{}_{cri} = 1.03$ C/cm^2 is the experimental $Q_p{}^{pri}$ at breakdown point when $(\iota^n/\iota^{pri}) * Q_n$ is negligible. When $Q_p{}^{pri}=0$, the experimental Q_n at breakdown point Q_{ncri} is 100 C/cm^2. Comparison of calculated curve by (1) with experimental data is in excellent agreement and therefore strongly support our simple model. $(\iota^{pri}/\iota^n) = Q_{ncri} / Q_p{}^{pri}{}_{cri} \approx 10^2$ indicates that hole is two orders of magnitude more effective than FN electron in causing oxide breakdown.

T3.4
A STUDY OF QUASI-BREAKDOWN MECHANISM IN ULTRA THIN GATE OXIDE UNDER VARIOUS TYPES OF STRESS. Hao Guan, Zhen Xu, Byung Jin Cho, M.F. Li and Y.D. He Department of Electrical Engineering, National University of Singapore, SINGAPORE.

The quasi-breakdown (QB) mechanism of ultra thin gate oxide is investigated through the observation of interface state generation during high field F-N stress and substrate hot hole and hot electron stresses. The interface state density was monitored using newly developed DCIV technique and charge pumping technique in dual

gate CMOSFET. During F-N stress, the interface state density is monotonically increased with stressing time until complete breakdown (CB) for thick oxides which does not show QB. In 3.5nm oxide, the interface state density is increased during stress, however saturated at the onset point of QB and keep constant until CB. Moreover, the saturation point is always the same even under different stressing conditions, while the charge-to-QB is an exponential function of gate voltage. This means that the QB is triggered when the interface state density reaches a certain critical value. In case of substrate hot carrier injection, it has been found that hot carriers are much more effective to trigger QB than F-N electrons at the same current level. Hot hole was found more effective than hot electron to trigger QB. These facts are explained with the effectiveness of interface state generation. The interface state density was monitored again during the hot electron or hole injection. It also has been found that the interface state density always has a constant value at the onset point of QB regardless of stress current density and stressing carrier types. All these results consistently support the interface damage model for the QB occurrence.

T3.5
INVESTIGATION OF QUASI-BREAKDOWN MECHANISM IN ULTRATHIN GATE OXIDES. Y.D. He, Hao Guan, M.F. Li, Byung-Jin Cho, and Zhong Dong*, CICFAR, Department of Electrical Engineering, National University of Singapore, SINGAPORE.
*Chartered Semiconductors Manufacturing Pte. Ltd, SINGAPORE.

This work investigates the quasi-breakdown (QB) mechanism in ultrathin gate oxides. Carrier separation experiments were conducted to CMOSFETs with 3.7 nm thick gate oxides. Constant current stresses for both polarities, i.e. gate and substrate side injections, were applied to n and p MOSFETs respectively. The evolutions of gate current I_g , source/drain current $I_{s/d}$, and substrate current I_{sub} before and after gate oxide QB were measured . Static carrier separation I-V measurements were taken right after QB. Our experimental results clearly show that QB is due to the formation of a local physically-damaged-region (LPDR) at Si/SiO_2 interface. At this region, the effective oxide thickness is reduced to the direct tunneling (DT) regime. The observed high gate current at low oxide field after QB is due to DT electron or hole currents through the region where the LPDR is generated. The $I_{s/d}$ and I_{sub} versus gate voltage curves were surprisingly analogous to those curves observed in fresh MOSFET with gate oxide of DT thickness. All experimental data can be explained in a unified way by the LPDR QB model and proper interpretation of the carrier separation measurements. Particularly, under substrate injection stress condition, there is several orders of magnitude increase of I_{sub} ($I_{s/d}$) at the onset point of QB for n (p) - MOSFET, which corresponds to valence electrons DT from the substrate to the gate. Consequently, cold holes are left in the substrate and measured as I_{sub} ($I_{s/d}$). These cold holes have no contribution to the oxide breakdown and thus the lifetime of oxide after QB is very long. Under gate injection stress condition, there is sudden drop and even change of sign of Isub ($I_{s/d}$) at the onset point of QB for n(p)-MOSFET, which corresponds to disappearance of impact ionization and appearance of hole DT current from the substrate to the gate.

T3.6
METAL OXIDE SILICON TUNNELING PHOTODETECTOR. C.W. Liu, M.H. Lee, I.C. Lin, W.T. Liu and W.S. Kuo, Dept of Electrical Engineering, National Taiwan Univ, Taipei, TAIWAN.

Both NMOS and PMOS photon detectors are demonstrated. An Al/2.3nm oxide/p-Si device with oxide grown by rapid thermal process at 900°C was fabricated. When the gate is biased at the positive voltage greater than threshold voltage in a NMOS tunneling diode, an inversion layer of electrons is formed at the oxide/p-silicon interface. As the positive gate bias increases, more and more electrons tunnel from the "incipient" inversion layer to the Al electrode through the thin gate oxide. Finally, the electron current saturates for the gate biased at a large enough voltage (0.3V), since the current is limited by the generation rate of the electrons in the inversion layer. When photons with energy larger than the bandgap illuminate on the diode, the photo generated electrons in the p-silicon can diffuse and be swept by electric field to the Al electrode by tunneling through the ultra thin gate oxide. The measured detection spectrum has a cut-off wavelength at 1.18 μm. The photo current increases with the light intensity and is relatively independent of the positive gate bias. The dark current can be reduced by a factor of 100 by increasing the growth temperature of rapid thermal oxide. A PMOS detector with oxide grown at the same temperature has similar dark current level, since the dark current is determined by the electron hole pair generation rate in the Si depletion region. The photo-generated holes can tunnel through the ultra-thin oxide and form the photo current. A large saturation voltage (2V) is observed in the PMOS due to the large valence band discontinuity, compared to NMOS.

T3.7
EVALUATION OF JTB-111 AND JTB-121 FOR PRE-GATE CLEANING. Gary Chen, Terry Gilton, Bob Carstensen, Whonchee Lee, Grady Waldo, and Gregory Mitchell, Micron Technology, Inc., Boise, ID; Wayne A. Cady, William C. Greiner IV, and Joseph M. Ilardi, Mallinckrodt Baker, Inc., Phillipsburg, NJ.

The RCA clean replacement materials, JTB-111 and JTB-121, which is a modified version of JTB-111, have been evaluated for pre-gate cleaning at Micron Technology, Inc. The one-step JTB-111 cleans yielded surface metal concentration, particle, silicon etching rate, and surface roughness comparable to the standard two-step, pre-gate cleaning process. A low-temperature JTB chemistry yielded good gate oxide integrity (GOI) data and showed a broad process window for JTB-111 in terms of chemical concentration, processing time, and temperature. The one-step JTB-111 pre-gate cleaning processes were tested on the 64 Mb DRAM manufacturing process. Yields were equivalent to those of the standard pre-gate cleaning process. However, the time to breakdown (ttb) of the JTB-111 clean was about 50% lower than that of the standard cleaning for certain test structures. With the JTB-121, the ttb was significantly improved to a level that was not statistically different from that of the standard pre-gate cleaning process.

T3.8
AN ALTERNATIVE METHOD FOR DECOUPLING THE $Si\text{-}Si0_2$ INTERFACE STATES AND THE OXIDE TRAPS. A. Benfdila and A. Chikouche, Microelectronics and Device Physics Lab, Electronics Insitute, University M. Mouloud of Tizi-Ouzou, ALGERIA.

The present paper proposes a method that can be used to separate the interface states present at the $Si\text{-}SiO_3$ from the oxide traps and the near interface states in the oxide.
The proposed method is based on current measurements performed using the Charge Pumping Technique as well as the Charge Extraction Technique [1]. The two current measurements are treated and analyzed and the different types of traps are defined and quantified.
In the purpose of studying the interface as well as the oxide traps in MOS device, an experimental set-up has been developed and the gate current is measured under different conditions of signal amplitude and frequency. This current measurement is named charge extraction technique [1]. The same current measurements are achieved using the charge pumping technique [2].
The experimental procedure consists of measuring the gate or substrate current of an MOSFET having its drain and source terminals unconnected [3]. The same measurement is repeated on the same device but having its drain and source connected to a reverse biasing voltage source. A gate voltage, in the form of a train of pulses, is applied to the MOSFET gate and the pulse base level is varied from accumulation to inversion levels. The pulse amplitude is chosen such that its bottom level is in the accumulation region and its top level in the inversion region. The signal frequency is chosen to give appreciable gate current under charge extraction process.
The current values obatined in the two different measurements are plotted with respect to the pulse base level of the gate signal. It has been noticed that the charge extraction current is maximum when the charge pumping current is minimum and vice versa.
It has been found the the charge pumping current is given by [2]:

$$I_{cp} = 2.q.A.f.D_{it}.kT\left[V_{th}.ni.\sqrt{\sigma_n\sigma_h} + Ln\left(\frac{V_{FB}-V_T}{V_G}\right)\sqrt{tt_f t_r}\right]$$

Where V_{FR} is the flatband voltage, V_T the threshold voltage V_G the amplitude of the pulse L_r and t_f the fall and rise times of the pulses, f the frequency of the signal, V_{th} the thermal velocity of electrons, n_i the number of available electrons, and σ_n is the capture cross section of carriers, Dit the density of the interface state, and A is the gate area.
The charge extraction current is given by [4]:

$$I_G = 2.q.f\left[\bar{D}_{it}\left(\Psi_B - 2.kT\left[\frac{\nu_{th}\sqrt{\sigma_n\sigma_p}n_i^2}{2.f.\sqrt{n_i.N_A}}\right]\right) + N_{ot.tot}.\left(1 - exp\left(\frac{-1}{f.\tau_{\nu f}}\right)\right)\right]$$

where Ψ_B the surface potential sweep, N_A the substrate concentration and, N_{ot} the density of the oxide traps, τ the trap time constant.
When the charge pumping current is maximum we notice that the charge extraction current is minimum. At maximum charge pumping current and for the low frequency case all the interface states and near interface states are exchanging carriers with the drain and source. This means that the gate current is only produced by the contribution of the oxide traps. In addition at higher frequencies, greater than 30 kHz, the near interface states do not follow the carrier exchange with the drain and source i.e., they are saturated and do not contribute to any current a formation. The gate current behavior was also found to be suitable for device characterization [5].
Moreover, when the charge pumping current is minimum, the charge extraction current is maximum and its formation include the

contribution of all the interface and oxide traps. It comes out that the combination of the expressions of I_{cp} and I_G and the current measurements at low and high frequencies can be used to separate the densities of the oxide traps, near interface traps and the interface states.

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T3.9

GATE INDUCED DRAIN LEAKAGE ENHANCED BY PLASMA CHARGING DAMAGE. Siguang Ma, Y.H. Zhang[1], M.F. Li , Weidan Li[2], J.L.F. Wang[1], Andrew C. Yen[1] and George T.T. Sheng[1], CICFAR, Department of Electrical Engineering, National University of Singapore, SINGAPORE. [1]Institute of Microelectronics, SINGAPORE. [2]LSI Logic Co., Santa Clara, CA.

Correlation between gate induced drain leakage current(GIDL) and plasma induced damage in gate oxide was investigated in MOSFETs with 5.0nm gate oxide. We measured the GIDL of pMOSFETs with same device structure but different location on the wafer and different ratio of attached antenna. The magnitude of the gate induced drain leakage current I_{GIDL} was found to increase monotonously with the increase of area ratio (AAR) or length ratio (ALR). On the other hand, I_{GIDL} changes regularly according to the distance between the device site and the center of the wafer: the larger the distance , the smaller the I_{GIDL} value. These facts imply that the increase in I_{GIDL} has close relationship with the gate oxide damage induced by plasma charging. The results of charge pumping (CP) measurement on the same devices revealed that the amount of interface states showed clearly the same trend with that of I_{GIDL} as a function of AAR, ALR or device location. Thus conclusion can be made that the increase in GIDL current is attributed to band-to-trap tunneling via interface traps introduced by plasma charging effect. This finding sets a new criteria of plasma induced damage. Since standby power dissipation is a crucial factor for thin-oxide MOSFETs, care should be taken of the effect of plasma charging not only for the reliability aspects, but also for the performance degradation of devices, especially performance in off-state. The threshold voltage (V_{th}) of different devices shows small variation regardless of the difference in AAR or ALR or location across the wafer, indicating oxide trapped charge by PID is negligible. Therefore, the conventional method using V_{th} shift as monitor is not enough and GIDL measurement is a necessary complementary tool for assessing deep submicron CMOS device performance degradation due to plasma charging damage.

T3.10

EFFECTS OF REVERSE BIASED FLOATING VOLTAGE AT SOURCE AND DRAIN ON THE PERFORMANCE OF NMOSFETS. D. Misra and R.K. Jarwal, Dept of Electrical and Computer Engineering, New Jersey Institute of Technology, University Heights, Newark, NJ.

We have examined the effects of reverse biased floating voltage at the source and drain on the performance of polycrystalline silicon and metal1 submicron n-channel MOSFETs with different antenna ratios. It has been established theoretically that the effective antenna ratio of an MOSFET increases with the reverse biased floating voltage at source and drain. Thus a small antenna ratio transistor with reverse biased voltage at source and drain behaves like a large antenna ratio transistor. This has also been verified experimentally for polycrystalline silicon and metal1 NMOSFETs with gate length of 0.35 micron and antenna ratios of 2009, 10066 and 50050 respectively.

T3.11

CHARACTERIZATION OF Ta_2O_5 THIN FILMS HAVING A SMALL LEAKAGE CURRENT FOR HIGH-DENSITY DRAMS. Naoki Kanda, Kiyoshi Ogata, Hitachi Ltd, Production Engineering Research Laboratory, Yokohama, JAPAN; Ryoichi Furukawa, Hirohiko Yamamoto, Masato Kunitomo, Yuzuru Ohji, Hitachi Ltd, Device Development Center, Tokyo, JAPAN; Masayoshi Ishibashi, Hitachi Ltd, Advanced Research Laboratory, Tokyo, JAPAN; Takuro Homma, Masato Takahashi, Hitachi Ltd, Semiconductor & Integrated Circuit Group, Tokyo, JAPAN; Toshio Uemura, Hitachi ULSI Systems Co., Ltd, Tokyo, JAPAN.

Ta_2O_5 was the first of the high-k materials to be applied in high-density DRAM capacitors. Although CVD-Ta_2O_5 film showed good thickness uniformity in Stacked Type Capacitors, the film had a somewhat large leakage current. Controlling the crystallization process of the film improved the leakage problem remarkably. The present study investigates the effects of crystallization and grain boundary on leakage current.
Ta_2O_5 thin films having thicknesses between 5 and 23 nm were deposited by the CVD method on polycrystalline Si substrates. The amorphous Ta_2O_5 thin films were crystallized by rapid thermal annealing. Two distinct crystallization behaviors were observed via X-ray diffraction measurements. In conventional films, the intensity ratio between 200 and 001 (I200/I001) was found to increase with an increase in film thickness. The intensity ratio of the improved films however was almost constant. In the improved films, the (200) and (001) oriented grains are believed to have grown together, forming harmonious grain boundaries. Observation via current-mode AFM confirmed the leakage current in the grain boundary of the improved films to be smaller than that of the conventional films.

T3.12

NEW WAFER CLEANING TECHNIQUE USING ELECTROLYTIC IONIZED WATER. Masako Kodera, Naoto Miyashita, Yoshitaka Matsui, Jun Takayasu, Toshiba Co., Manufacturing Engineering Center, Yokohama, JAPAN; Soichi Nadahara, Hiroshi Tomita, Toshiba Co., Microelectronis Center, Yokohama, JAPAN.

It is known that the conventional RCA cleaning is effective to remove metal contamination, however, relatively large amount of chemical usage is necessary for the RCA cleaning, which requires higher capacity of the waste chemical treatment system, and also influence of the chemicals on environment has been an issue needed to be considered. Experiments on performance of the cleaning wafers with the electrolytic ionized water were performed, and the results confirmed that the new cleaning technique was as effective as the RCA cleaning. Contaminated wafers were subject to cleaning with diluted HF followed by cleaning with anode water, and it was confirmed that metal contamination on the wafers were reduced below detection limit of the ICP-Mass. Also, based on results of the lifetime measurement tests on the devices on the cleaned wafers, which was performed to evaluate influence of metal contamination on the device characteristics, it was confirmed that; 1) the devices cleaned with the anode water had a lifetime equivalent to or longer than the devices cleaned with the RCA; 2) the ionized waster had high effectiveness to remove metal contamination; and 3) metal contamination removed from the wafer did not go back to the wafer. Moreover, results of evaluation on reliability showed that cleaning with the ionized water had effective performance equivalent or superior to RCA cleaning.

T3.13

MECHANISM OF ELECTROLYTIC IONIZED WATER CLEANING FOR POLY SILICON CMP PROCESS. Naoto Miyashita, Masako Kodera, Jun Takayasu, Yoshihiro Minami, Yoshitaka Matsui, Masahiro Abe, Kouichi Takahashi, Toshiba Co., Manufacturing Engineering Center, Yokohama, JAPAN; Satoko Iwami, Takeshi Nishioka, Toshiba Co., Mechanical System Laboratory, Kawasaki, JAPAN.

Chemical-Mechanical-Polishing has been revealed as an attractive technique for poly Si of trench planalizing process. Major issue of the process integration is post-CMP cleaning process. A new post CMP cleaning process which employed eletrolytic ionized water has been reported in this paper. In general, wafers after CMP process are contaminated by particles and metallic impurities in the case of conventional cleaning method. The contamination introduce the defects into the wafers after oxidation. The new cleaning method removed the contamination, using electrolytic ionized water containing a small quantity of chemicals. The anode water have the effect of cleaning metal and organic contamination, and the cathode water have the effect of removing particles and etching poly Si surface. This new cleaning process is useful for CMP process and makes the impurity level very low. The experimental wark has focused on critical problems that had to be solved, which has been examined by AFM, EDX, and VPD-ICP/MS.

T3.14

DIELECTRIC PROPERTIES OF THE $Bi_2Ti_2O_7$ THIN FILM WITH (111) ORIENTATION. Zhuo Wang[1,2], J. Huang[3], X.M. Wu[1,2], H. Wang[1,2], M. Wang[1,2], and S.X. Shang[1]; [1]State Key Lab. of Crystal Materials; [2]Institute of Crystal Materials, Shandong University, Jinan, CHINA; [3]Department of Environment and Engineering,Shandong University, Jinan, CHINA.

The $Bi_2Ti_2O_7$ thin films have been prepared on silicon by metalorganic decomposition (MOD) technique using bismuth nitrate and titanium butoxide as source materials. The growth procedure of the $Bi_2Ti_2O_7$ thin films was discussed. The surface morphology of the $Bi_2Ti_2O_7$ film was studied by using the Electric Force Microscope (EFM). The crystallization of the films was studied by x-ray diffraction (XRD) using a Rigaku D/MAX-(A x-ray diffractometer.

The $Bi_2Ti_2O_7$ thin film prepared on (100) silicon substrate was proved with strong (111) orientation. The dielectric properties of the $Bi_2Ti_2O_7$ films measured by HP 4192 Impedance Analyzer and current-voltage (I-V) characteristics measured by HP4140B PA meter. The dielectric constant of the $Bi_2Ti_2O_7$ thin films vs the temperature and frequency in the interval 100-800°C were studied. The dielectric constant and dielectric loss were found to be 118 and 0.07 respectively in 100KHz at room temperature. The resistivity of the $Bi_2Ti_2O_7$ thin film is higher than 1×10^{12} (Ω·cm) under the applied voltage from -5V to 5V. The $Bi_2Ti_2O_7$ thin film is about 0.4 μm-thick film annealed at 500°C for 30 minutes, its leakage current density was 4.06×10^{-7} A/cm^2 at the applied voltage of 15V. This shows the films have very good insulating property. Recently there is tremendous interest in using high dielectric constant materials for storage capacitors in dynamic random access memory (DRAM) application and as gate insulators to increase the transconductance of MOSFET.

T3.15
ULTRA THIN NO/N2O OXYNITRIDE DIELECTRIC FOR ADVANCED FLASH MEMORY APPLICATION: SINGLE WAFER AND BATCH TECHNOLOGY. B. Crivelli, R. Zonca, M.L. Polignano, F. Cazzaniga, M. Alessandri, STMicroelectronics, Agrate, ITALY; A.P. Caricato, INFM-MDM, ITALY; M. Bersani, M. Sbetti, L. Vanzetti, ITC-IRST, Povo di Trento, ITALY; G.C. Xing, G.E. Miner, S. Nesso, N. Astici, S. Kuppurao, D. Lopes, Applied Materials, Santa Clara, CA.

In VLSI technology, N2O/NO nitrided oxides are considered as feasible candidates for gate application in 0.18 micron CMOS generation and beyond. This paper presents an exhaustive and systematic investigation of nitrided oxides obtained by Rapid Thermal Oxidation/Nitridation in AMAT Centura System considering two different aspect: first the comparison between single wafers and batch technology, second the different possible oxide architecture achievable with RTO/RTN system (i.e. RTO + RTN, RTN + RTO, RTN + RTO + RTN). The samples were analyzed by means of SIMS, XPS, ELYMAT, AFM and Etching Rate study. For the first part of the work, 50 A wet oxidations (ISSG, In Situ Steam Generator) followed by N2, N2O and NO annealing where compared. In RTO/RTN case, the nitrogen content and its within wafer uniformity were found to be different with respect to the ones achieved with standard batch technology. Moreover, on the contrary of what observed on furnaces processes, the N profile and chemical environment inside the oxide did not differ significantly varing the nitridation ambient, i.e. NO vs N2O. For the second part of the work, 30 and 50 A oxides where studied considering post-oxidation annealing or reoxidation of native oxide nitrided by NO. Both dry and wet oxidations were taken into account: the presence of high concentration of atomic oxygen in the ISSG process with respect to dry one seems to affect the N distribution and bonding in the films and the quality of the pure oxide itself. Moreover for wet process, the physical results were correlated with electrical data obtained on MOS capacitors: the film obtained performing a NO RTN nitridation of the native oxide followed by a ISSG oxidation exhibited very promising electrical properties (higher Qbd values under both polarity injection and lower defectivity) that made it an appealing candidate as gate dielectric in CMOS and Flash memories applications.

T3.16
EVALUATION OF THE DEGRADATION DYNAMICS OF THIN SILICON DIOXIDE FILMS USING MODEL-INDEPENDENT PROCEDURES. R. Rodriguez, M. Nafria, E. Miranda, J. Sune and X. Aymerich, Dept. Enginyeria Electronica, Universitat Autonoma de Barcelona, Bellaterra, SPAIN.

The degradation and breakdown of thin silicon dioxide films has been analysed using a recently presented two-step stress method. By provoking the oxide breakdown in two stages (pre-stress and final breakdown test), the method allows the evaluation of the degradation induced by the electrical stress looking at the evolution of the breakdown statistics, without any assumption about the microscopic nature of the degradation process. The degradation dynamics in constant-voltage (CVS) and constant-current stresses (CCS) has been analysed and compared using this method. In both kind of tests, the degradation rate and the mean-time-to-breakdown show the same exponential dependence on the stress voltage, pointing a clear relation between degradation and breakdown. However, while in CCS the degradation proceeds till the occurrence of breakdown, in CVS the degradation tends to saturate (significantly before the oxide failure). This observation suggests that, in CVS, the degradation leading to breakdown occurs in two stages with quite different time constants. From the fitting of the current-time characteristics (I-t) of virgin capacitors, it has been observed that, in the case of the considered oxides (8nm thick), both degradation stages have an effect on the current evolution during the stress. The experimental characteristics have been correctly fitted to the superposition of three exponential components, with three different time-constants. However, most of the I-t curve is controlled by just two of the components, whose time constants show a striking coincidence with the degradation rate (obtained using the two-step stress method) and the time-to-breakdown measured on virgin oxides. This result suggests a very fast tool for the reliability evaluation of thin oxides: the fitting of the I-t characteristics to estimate the degradation rate (without any assumption about the nature of the degradation process) and the mean-time-to-breakdown.

T3.17
STEREOCHEMICAL STRUCTURE FOR SODIUM IN NATIVE AND THERMAL SILICA LAYERS. Anne Marie Flank, Francois Tenegal, Pierre Lagarde, Lure, Orsay, FRANCE; Cristophe Mazzara, Jacques Jupille, Laboratoire CNRS-Saint-Gobain, Aubervilliers, FRANCE.

Little being known about the chemical environment of the sodium in the soda-silica glass, in particular regarding its respective bonding to bridging and non-bridging oxygen atoms, a suggestion has been to examine the behaviour of alkali metal atoms deposited onto pure silica, which is expected to mostly involve bridging oxygen atoms. We present herein an ultra-high vacuum study, by X-ray photoemission spectroscopy (XPS) and X-ray absorption spectroscopy (EXAFS), of sodium-covered native and thermal silica layers grown on a Si(100) wafer. It is shown that the sodium diffuses on a reversible manner within the silica layer at 300 K. The presence of sodium results (i) in an about 1.6 to 2.2 eV shift of the O 1s core level with respect to the bulk silica, analogous to the shift characterizing non-bridging oxygen in soda-lime glass and (ii) in a near edge structure and an EXAFS spectrum similar to those of glass. Moreover, it is established that the chemical environment of sodium involves defined first and second interatomic distances which compare within one to two per cent to those observed in glass. This proves that a sodium atom incorporated into the silica network builts up a specific site and indicates that, at variance with existing models, the alkali ions used as network modifiers elements in glass making might have a significant influence on the structure of the material.

T3.18
CHEMICAL AND STRUCTURAL CHARACTERIZATION OF ULTRATHIN DIELECTRIC FILMS USING AEM.
John Henry J. Scott, Eric S. Windsor, Dale E. Newbury, National Institute of Standards and Technology, Gaithersburg, MD.

The structure and chemical heterogeneity of ultrathin silicon oxide and silicon oxynitride films, used as gate dielectrics in semiconductor electronic devices, are studied using analytical electron microscopy (AEM). Laterally homogeneous blanket films varying in thickness from 4 nm to less than 2 nm are characterized in cross section using a 300 keV field emission TEM/STEM equipped with energy-dispersive x-ray (EDS) and electron energy-loss spectrometers (EELS). High resolution imaging (HRTEM) supported by multislice HRTEM image simulation is used to investigate the accuracy and precision of film-thickness measurements and their comparability to other techniques such as secondary ion mass spectrometry, spectroscopic ellipsometry, x-ray reflectivity, and medium energy ion scattering. In STEM mode, the AEM is used to probe the chemistry of the sample at very fine length scales. Powerful new automation procedures allow the collection of multiple analytical signals simultaneously (e.g. annular dark field STEM, EDS, and EELS) during scanned-probe image acquisition. The use of hyperspectral imaging techniques, such as EDS and EELS spectrum profiling, for extraction of composition and chemical bonding information is also presented.

T3.19
CHARACTERIZATION OF ULTRATHIN SILICON-OXYNITRIDE FILMS USING GRAZING INCIDENCE X-RAY PHOTOELECTRON SPECTROSCOPY. E. Landree, and T. Jach, Surface and Microanalysis Science Division, National Institute of Standards and Technology, Gaithersburg, MD.

Incident monochromated X-rays that impinge upon a smooth surface at angles less than the critical angle (typically about 0.7 degrees for 1820 eV incident X-rays on silicon) undergo total external reflection. By varying the angle of the incident X-rays relative to the sample surface it is possible to control the X-ray penetration depth within the sample. The emitted photoelectrons can then be measured for varying angles of incidence to determine properties such as the sample composition, structure profile and local chemical bonding as a function of depth. This method of using grazing incident X-ray photoemission spectroscopy (GIXPS) offers several advantages for the characterization of ultrathin oxynitride films on silicon. Within an X-ray energy range of 1-2 keV, the limit of the electron mean free path in the film makes this technique particularly well suited for characterizing films on the order of 4 nm thick or less. In addition, GIXPS is chemically sensitive to photoelectrons that emanate from silicon in the bulk and silicon in the dielectric film. Utilizing the

non-linear dependence of the photoelectron yield upon quantities such as film thickness, density, cross-section, index of refraction, and electron mean free path, one is able to construct a model of the film profile to describe the observed data. An additional advantage is that GIXPS is a standardless technique, and therefore dependents only upon the specific material constants. It also provides a non-destructive means of characterizing the films of interest. The merits of different profile structures will be illustrated and the obtained dielectric film thickness will be compared to results obtained using other available techniques including transmission electron microscopy, spectroscopic ellipsometry and x-ray reflectivity.

T3.20
ANALYSIS OF MOS DEVICE CAPACITANCE-VOLTAGE CHARACTERISTICS BASED ON THE SELF-CONSISTENT SOLUTION OF THE SCHRODINGER AND POISSON EQUATIONS. Christophe Raynaud, Jean-Luc Autran, Alain Poncet, LPM, INSA de Lyon, Villeurbanne, FRANCE.

As the dimensions of semiconductor devices commonly used in microelectronics further decrease, scaling rules involve higher doping levels and thinner oxide layers. This leads to higher electric fields at the oxide/silicon interface and to a narrowing of the inversion and accumulation layers. Therefore, quantified energy levels appear in these potential wells. The carrier density is thus modified with regard to the classical model. In the past, several works have determined capacitance-voltage (CV) characteristics by solving the Schrödinger's and Poisson's equations (SP model) [1,2] or by using a first order correction for quantum effects [3]. In this paper, we investigate these two different approaches to take into account the quantum effects in the calculation of the CV characteristics of metal-oxide-semiconductor (MOS) structures. In the accumulation regime, the majority carrier density has been considered as the superposition of both carrier populations issued from the continuum of states and from the first quantified levels at the interface. We first solve numerically both the Schrödingers and Poisson's equations using a three-point finite difference scheme with a non-uniform mesh size to obtain the potential bending and the charge in the quantum well. After showing that taking into account the three deepest quantified levels is sufficient, we compare these results with the charge densities obtained with the Boltzmann's statistic with and without a first order quantum effect correction and with the exact Fermi-Dirac statistic. Then the complete calculation of the CV characteristics allows to quantify the errors made by the different approaches in determining the oxide thickness from CV measurements (for different thickness ranging from 2 to 8 nm). [1] Y. Ohkura. Solid-State Electronics, 33, 1581 (1990). [2] J.A. Lopez-Villanueva, I. Melchor, F. Gamiz, J. Banqueri and J.A. Jimenez-Tejada. Solid-State Electronics, 38, 203 (1995). [3] R. Rios and N. Arora. IEDM Tech. Dig. Dec., 613 (1994).

T3.21
ROOM TEMPERATURE ULTRAVIOLET PHOTOLUMINESCENCE FROM 800°C THERMALLY OXIDIZED $Si_{1-x-y}Ge_xC_y$ THIN FILMS ON Si (100) SUBSTRATE. Xuemei Cheng, Youdou Zheng, Lan Zang, Xiabing Liu, Shunming Zhu and Zhiyun Lo, Physics Dept, Nanjing Univ, Nanjing, CHINA.

During the last few years, special interest has been devoted to photoluminescence of oxidized silicon based materials. However, to our best knowledge, studies on the room temperature photoluminescence characters of the thermally oxidized $Si_{1-x-y}Ge_xC_y$ thin films have never been reported yet. In this letter, we report that photoluminescence of thermally oxidized $Si_{1-x-y}Ge_xC_y$ thin films on Si (100) substrates were observed at room temperature. The $Si_{1-x-y}Ge_xC_y$ thin films rich in Ge and C content were grown on Si(100) substrate by Plasma enhanced Chemical Vapor Deposition (PECVD) and then wet oxidized at 800°C. Photoluminescence spectra of the samples were measured at room temperature under 250nm excitation. Two ultraviolet photoluminescence bands with the peaks at ~370nm and ~396nm were observed in the oxidized samples. Photoluminescence Excitation (PLE) spectroscopy, Auger Electron Spectroscopy (AES), and X-ray Photoelectron Spectroscopy (XPS) were used to analyze the microstructures and study the photoluminescence mechanism of the samples. We attributed the 396nm band to the defects O-Si-O or O-Ge-O in the oxidized films, while the 370nm band was related to C in the films.

T3.22
AN XPS STUDY OF SILICON DIOXIDES RAPID THERMALLY GROWN IN OXYGEN, NITROUS OXIDE AND NITRIC OXIDE. W. H. Lai, M F. Li, National University of Singapore, Dept of Electrical Engineering, SINGAPORE; J.S. Pan, National University of Singapore, Surface Science Lab, Dept of Physics, SINGAPORE; L. Chan, R & D Dept, Chartered Semiconductor Manufacturing Ltd, SINGAPORE; T.C. Chua, Applied Materials South-East Asia Pte Ltd, SINGAPORE.

Earlier RTO growth studies were limited in the process conditions employed, temperature measurement uncertainty, and thermal non-uniformity across the wafer. Using a state-of-the-art RTP system, the RTO growth characteristics in oxygen, nitrous oxide and nitric oxide were investigated. Anomalies including higher growth rates at a lower pressure in nitrous oxide, higher growth rates at lower temperatures and at a lower pressure in nitric oxide, as well as higher growth rates in nitrous oxide and nitric oxide than in oxygen were observed. XPS was used to determine the correlation between these anomalies and the bonding structures in the oxides.

T3.23
IMPROVED PERFORMANCE AND RELIABILITY IN AGGRESSIVELY-SCALED pMOS AND nMOS FETs WITH i) ~0.6 nm MONOLAYER NITRIDED OXIDE INTERFACES AND ii) OXIDE-EQUIVALENT THICKNESSES TO 1.3 nm BY REPLACEMENT OF PLASMA-PROCESSED STACKED OXIDE/NITRIDE DIELECTRICS WITH HOMOGENEOUS OXYNITRIDE ALLOYS. Hanyang Yang, Hiro Niimi and Gerald Lucovsky, NC State Univ, Raleigh, NC.

Model calculations, which assume a linear variation in the dielectric constant with alloy composition, have been used to compare direct tunneling in gate dielectrics with the same oxide-equivalent thickness, tox-eq, across the pseudo-binary join-line form SiO_2 to Si_3N_4. Interfacial barrier heights. E_{bx}, and electron tunneling masses, m_x*, have been obtained for end-member oxides, o, and nitrides, n, by analysis of tunneling in devices with oxide and stacked oxide/nitride gate dielectrics prepared by remote plasma-processing. The conduction band offset energies obtained in this way are E_{bo} = 3.15 eV and E_{bn} = 2.15 eV, and the tunneling masses are m_o* = 0.55 m_o and m_n* = 0.25 m_o. If it is further assumed that E_{bx} and m_o* vary linearly with N-content, then the optimum dielectric for tunnel current reduction for fixed tox-eq is not the end-member nitride, but rather a high N-content oxynitride alloy (0.5). This model has been tested and verified in devices with nitride and oxynitride gate dielectrics prepared by plasma-assisted processing. Test devices included an ~0.6 nm interfacial nitrided oxide prepared by remote plasma-assisted oxidation, followed by remote plasma-assisted interface nitridation. For devices with these nitrided interface layers, tunneling data for oxide, oxynitride and nitride dielectrics could be directly compared, confirming model predictions that minimization of direct tunneling is obtained in devices with oxynitride alloys with N to O-atom ratios ~2, or equivalently at a pseudo-binary alloy composition of $(SiO_2)_{0.5}(_3N_4)_{0.5}$. These oxynitride layers have been integrated into PMOS and NMOS FETs, and their performance and reliability have been found to be improved with respect to devices with the same tox-eq employing stacked oxide-nitride gate dielectrics. Supported by NSF, SRC, and ONR

T3.24
STRUCTURE ANALYSIS OF $CeO_2/ZrO_2/Si$ MULTILAYER THIN FILMS BY HRTEM. Takanori Kiguchi, Naoki Wakiya, Kazuo Shinozaki and Nobuyasu Mizutani, Tokyo Institute of Technology, Dept of Metallurgy and Ceramics Science, Tokyo, JAPAN.

The structure and orientation relationships of the epitaxial $CeO_2/ZrO_2/Si$ and $ZrO_2/CeO_2/Si$ multilayer thin films are investigated by high resolution transmission electron microscopy (HRTEM). In the case of $CeO_2/ZrO_2/Si$, the CeO_2 layer on the ZrO_2 one has strong epitaxial structure with <100> orientation, although the epitaxy of the ZrO_2 layer is out of order from the <100> orientation. On the other hand, in the case of $ZrO_2/CeO_2/Si$, the epitaxy of both the layers is out of order from the <111> orientation. The difference of these multilayer thin films is considered.

T3.25
CONTROLLING THE CONCENTRATION AND POSITION OF NITROGEN ULTRATHIN OXYNITRIDE FILMS BY USING RADICAL OXYGEN AND NITROGEN. Koji Watanabe, Koji Watanabe, Toru Tatsumi, NEC Corporation, Silicon Systems Research Laboratories, Tsukuba, JAPAN.

Oxynitride films are useful for making high-quality metal-oxide-semiconductor gate insulators. In particular, they suppress boron penetration and reduce hot-carrier damage. These performances depend on the concentration and position of nitrogen in the film, hence, it is important to control these parameters of nitrogen. We used radical oxygen and nitrogen from an electron-cyclotron resonance (ECR) plasma to form an ultrathin oxynitride film in an ultrahigh vacuum (UHV) system. This system allowed us to easily keep the oxynitride thickness to less than 2.0 nm. We also expect to form a high-density film by using radical species because the leakage current depends on the density. We treated 8-inch Si(100) wafers by SC-1 cleaning followed by HF dipping. After that, the oxynitride films were formed by using three processes: (a) radical nitridation after radical oxidation, (b) radical oxidation after radical

nitridation, and (c) supplying radical oxygen and radical nitrogen simultaneously. We investigated the nitrogen concentration, nitrogen position, and interface roughness of the films and found that the N concentration can be controlled to between 0 and 15%. Although the interface roughness tends to increase with the N concentration, supplying radical oxygen and nitrogen simultaneously decreases the roughness and increases the nitrogen concentration in the film (N: 12.1%, RMS: 0.12 nm). A high amount of nitrogen is needed to protect the boron diffusion. However, the electron mobility depends on the interface roughness, and it decreases due to interface scattering as the interface roughness increases. Therefore, supplying radical oxygen and nitrogen simultaneously is the best way to decrease the roughness and increase the nitrogen content of the film. We also found that the nitrogen position can be controlled from near the surface to close to the interface by using three processes. Radical oxynitridation should thus be very suitable for fabricating ultrathin gate-insulator films.

T3.26
MODIFICATION OF MOS STRUCTURE PARAMETERS UNDER ARC PLASMA JET TREATMENT. Vladimir V. Andreev, Bauman Moscow State Technical University, Kaluga, RUSSIA; Vladimir M. Maslovsky, Zelenograd Research Institute of Physical Problems, Moscow, RUSSIA; Anton A. Obednin, Mikron Corporation, Moscow, RUSSIA; Georgy Ya Pavlov, JSC Concern Scientific Center, Moscow, RUSSIA.

In the presented work for modification of parameters MOS structures the new technology APJT (arc plasma jet treatment) was used. The distributions of the initial parameters of the Si/SiO_2 structures were homogeneous across the wafer surfaces and similar for all the wafers. The width of oxide made 90 cm^{-11}. The parameters were as follows: breakdown voltage V_{bd} = 20 to 21 V (breakdown field E_{bd} = 8 MV/cm); charge stability Q_{bd} = 0.3 to 0.5 C*cm^{-2}. After APJT, the electrical parameters of the structures remained uniform across the surface. We showed that this APJT has no essential effect neither on the C-V characteristics, nor on N_{ss} and n. After APJT typical time variation of leakage voltage (the voltage on MOS structure that corresponds to a constant current of 50 μA passing through the oxide) increased noticeably (by 1.5 to 4 times). The breakdown field E_{bd} increased to above 30 MV/cm. Other initial structure (100 chips per wafer) had low charge stability. The width of oxide made about 25 cm^{-11}. With increasing APJT time, the fraction of chips with low Q_{bd} (<0.5 C*cm^{-2}) decreased and the fraction of high-Q_{bd} chips (>5 C*cm^{-2}) increased.

T3.27
CORRELATION BETWEEN DEVELOPMENT OF LEAKAGE CURRENT AND HYDROGEN IONIZATION IN ULTRATHIN SILICON DIOXIDE LAYERS. Valery Afanas'ev and Andre Stesmans, University of Leuven, BELGIUM.

The generation of leakage current across 3-6-nm thick thermal oxides on (100)Si under electrical stress or irradiation with 10-eV photons is compared with the radiation-induced defect generation in 35-66-nm thick oxides. The degradation of both ultrathin and thick oxides appears correlated with the concentration of atomic H in the layer. Both the leakage currents and the irradiation-induced defect states were found to have two components: First, there is a thermally unstable leakage current that correlates with the generation of the H-induced donor states, and, second, there is a stable leakage current corresponding to the permanent oxide damage and correlated with bond break in the oxide, revealed by ESR analysis as the H-stimulated generation of E-centers. This correlation importantly indicates that the same degradation mechanisms account for the radiation induced damage of both ultrathin and thick oxides. Additionally, a strong similarity is observed between the leakage currents after electrical stress and 10-eV photon exposure, indicating that the hole generation or injection into the oxide is not the principal cause of the damage in the ultrathin oxides. We suggest that the atomic hydrogen introduced into the oxide during stress or irradiation is ionized by emitting electrons from the energy level of the H-induced donor state (at 0.25 eV above Si midgap) to the Si or to the gate electrode. Upon H ionization, the oxide degradation proceeds in the same was as upon irradiation. Therefore, no separate hole injection mechanism is required to account for positive charging and bond break in ultrathin oxides during electrical stress.

T3.28
FROM RADIATION INDUCED LEAKAGE CURRENT TO SOFT-BREAKDOWN IN IRRADIATED MOS DEVICES WITH ULTRA-THIN OXIDES. Marco Ceschia, Alessandro Paccagnella, Universita di Padova, Dipartimento di Elettronica e Informatica, Padova, ITALY; Gabriella Ghidini, ST Microelectronics, Agrate Brianza, ITALY; Jeff Wyss, Universita di Cassino, Cassino, ITALY.

MOS capacitors with ultra-thin oxide and nitrided oxide layers have been irradiated with ionising particles (8 MeV electrons or Si, Ni, and Ag high energy ions), featuring a variety of LET values. Different oxide fields (Fbias) have been applied during irradiation, ranging between flat-band and 4 MV/cm. After irradiation, we measured the DC Radiation Induced Lekage Current (RILC) at low fields (3-6 MV/cm). RILC can be modeled as a trap-assisted tunnelling current, with electrical characteristics similar to those of the SILC measured after electrical stresses. For all LET values, RILC increased almost linearly with the total radiation dose up to very high doses (150 Mrad(Si)). This characteristic is strikingly different from the growth rate observed under electrical stresses, which is sublinear with the injected charge. These results indicate different accumulation rates of oxide defects mediating RILC/SILC and suggest possible clues on the mechanisms of defect generation and passivation under stress. Further, Fbias affects RILC, but a strong dependence on the radiation LET is observed. At relatively low LET values (<9 MeV·cm^2/mg), RILC is maximum for flat band Fbias, and it decreases if Fbias increases. For high LET values (>25 MeV·cm^2/mg), the opposite is measured. Moreover, at high LET and Fbias, the RILC Ig-Vg curves present the noisy features proper of Soft-Breakdown curves, pointing to a transition from RILC to Soft-Breakdown mediated by the field applied during the stress. The role of positive trapped charge in generating the oxide defects will be addressed as well.

T3.29
HIGH QUALITY ULTRA-THIN SILICON DIOXIDE FILMS FORMED BY DIRECT OXIDATION IN A Cat-CVD SYSTEM. Manabu Kudo, Akira Izumi, Hideki Matsumura, JAIST (Japan Advanced Institute of Science and Technology), School of Materials Science, Ishikawa, JAPAN.

Ultra-thin silicon dioxide films can be formed as a gate insulator at temperatures as low as 300°C by direct oxidation of Si. In such a direct oxidation, active oxygen species generated by a tungsten catalytic reaction in a catalytic chemical vapor deposition (Cat-CVD) system is utilized. In this catalytic cracking oxidation (cat-oxidation), the electrical properties of films appear to depend on the existence of very thin pre-oxide layer on Si surface before cat-oxidation. In this paper, the effect of pre-oxide is investigated in order to improve the electrical properties of cat-oxidation films. 0.6nm-thick pre-oxide on Si surface is formed by chemical treatment in a mixed solution of H_2SO_4 and H_2O_2 (H_2SO_4:H_2O_2=4:1) at 90°C for 10min. Silicon dioxide films of total thickness of 2nm is formed on the pre-oxide substrate at temperatures around 300Å irradiating active oxygen species generated by catalytic decomposition of H_2O on heated tungsten in a Cat-CVD system. The electrical properties of such ultra thin silicon dioxide films are investigated. It is found that the breakdown electric field is larger than 13 MV/cm and leakage current is around 3Å $\sim 10^{-9}$ A/cm^2 for the applied electric field of 1MV/cm, which is much better than thermally growth silicon dioxide at 1000°C. The results indicate that ultra-thin silicon dioxide films, formed at temperatures as low as 300°C by direct oxidation in a Cat-CVD system, is promising as a new gate insulator in ULSI when pre-oxide layer on Si surface is chemically formed before oxidation.

T3.30
TEMPERATURE AND FIELD DEPENDENCE OF STRESS INDUCED LEAKAGE CURRENTS IN VERY THIN GATE OXIDES. Didier Goguenheim, Alain Bravaix, Bouchra Ananou, ISEM-LEMMI, Toulon, FRANCE; Franáois Mondon, Gilles Reimbold, CEA-LETI, Grenoble, FRANCE.

We have precisely investigated the temperature and field dependence of Stress Induced Leakage Currents (SILC) that appear at low field through the SiO_2 oxide of MOS devices (capacitors and MOSFET's) after high field stresses. Two oxide thicknesses were available (4.7 and 3.8 nm) on P-Si substrates and three stressing modes were used: Constant Current Stresses (CCS) or Constant Voltage Stresses (CVS) with electrons uniformly injected from the N+ poly-Si gate and localized channel hot-hole (CHH) injections in MOSFETs. The creation kinetics of these SILC follows a typical power law with a degradation rate practically independent of the thickness and of the stressing conditions in capacitors (CVS or CCS) [1]. No evidence of a positive charge trapping is found and no significant difference is found between CVS and CCS modes. A smaller slope in the time power law is observed for CHH degradations [2]. In contrast to previous results, a Fowler-Nordheim component with a reduced barrier height does not fit correctly the voltage dependence of SILC, which seems to be better described by a Schottky-like or Poole-Frenkel law in 4.7nm-thick samples, more poorly in 3.8nm-thick oxides [2]. On the other hand, we show that SILC currents exhibit a very low thermal activation in the 100-400K range with an activation energy less than 50 meV in 4.7nm oxides and less than 20 meV in 3.8nm oxides. This result rules out the possibility of a thermoionic law. All these facts, enhanced by the fundamental exponential dependence of SILC with the applied field, are in favor of a trap assisted tunnel process (elastic or inelastic [3]) as being the mechanism responsible for SILC, which will be further

examined at the conference. [1] A. Scarpa et al., Microel. Engineering, 36, p.145 (1997) [2] D. Goguenheim et al., Journal of Non-Crystalline Solids, vol. 245, p.41 (1999) [3] B. Ricco et al., IEEE Trans. on Electron Dev., vol.45, No.7, p.1554 (1998)

T3.31
NITRIDE AND OXYNITRIDE OF SILICON FOR FUTURE ULTRA-THIN DIELECTRIC APPLICATIONS. Sanjit Singh Dang and Christos G. Takoudis, Advanced Materials Research Laboratory, Department of Chemical Engineering, University of Illinois at Chicago, Chicago, IL.

Ultra-thin silicon nitrides and oxynitrides are being studied for use in complementary metal oxide semiconductor field effect transistors (for Si-based microprocessors), dynamic random access memories (for data storage devices), and optoelectronic integrated circuits (for optical waveguide applications). Nitrogen incorporation in these films is critical to attain much better characteristics than silicon dioxide, especially when the film thickness is less than about 5nm. In this study, focus is on control of the electrical properties with variations in chemical composition and state. Bonding states in the films were studied using x-ray photoelectron spectroscopy while depth profiling of N and O was done using secondary ion mass spectrometry. Film thickness and refractive index were measured using spectroscopic ellipsometry. Using the data obtained, efforts are directed towards developing these materials with as high nitrogen content as possible for future high-k dielectric applications.

T3.32
STRUCTURAL, OPTICAL AND ELECTRICAL CHARACTERISTICS OF SILICON CARBON NITRIDE. L.C. Chen, C.Y. Wen, C.T. Wu, National Taiwan University, Center for Condensed Matter Sciences, Taipei, TAIWAN; J.-J. Wu, K.H. Chen, Academia Sinica, Institute of Atomic and Molecular Sciences, Taipei, TAIWAN; W.T. Liu and C.W. Liu,National Taiwan University, Department of Electrical Engineering.

Dielectric layers of thin silicon carbon nitride (SiCN) films have been deposited by electron cyclotron resonance plasma chemical vapor deposition (ECRCVD) and ion beam sputtering deposition (IBD) techniques. For submicron MOS device applications, a low interface roughness, a proper dielectric constant and a low current leakage in the gate dielectrics of reduced thickness are important. We address these aspects for the SiCN thin films deposited on p-type Si and present their structural, optical and electrical characteristics as a function of the deposition conditions. Spectroscopic ellipsometric analyses of the films indicated that the refractive index (and the derived dielectric constant) of the SiCN was comparable with silicon nitride and could be adjusted by varying the composition of SiCN films. For electrical measurements, Al gate electrodes were fabricated on the SiCN films to form metal-SiCN-silicon diodes. Preliminary studies of SiCN films deposited at low temperatures (e.g., 250 degree C by ECRCVD and room temperature by IBD) have already shown promising performance. The SiCN films deposited by ECRCVD exhibited low leak currents up to an applied field of about 2 MV/cm whereas the SiCN films deposited by IBD showed a somewhat higher leak currents without breakdown within our measured range. For large positive gate bias, the current was limited by the thermally generated electrons in the p-type Si substrates, and was independent of the gate bias and the film thickness. For negative gate bias, the electrons in the Al electrode tunneled through the traps in the SiCN film (Frenkel-Poole type), and the current level was relatively independent with the film thickness. These traps may be due to the extremely low growth temperature of these novel films. The electrical properties of the SiCN films grown at higher temperatures will also be reported.

T3.33
NANOSCALE SILICON FEATURES PRODUCED BY SLOW HIGHLY CHARGED IONS. M.W. Newman, A.V. Hamza, H. Lee, A.V. Barnes, T. Schenkel, J.W. McDonald, G.A. Machicaone, T. niedermayr and D.H. Schnieder Lawrence Livermore National Laboratory, Livermore, CA.

Phase transformations induced by intense, ultrafast electronic excitation from slow highly charged ions from the Lawrence Livermore National Laboratory (LLNL) Electron Beam Ion Trap(EBIT) have been studied. A 308 keV beam of Xe^{44+} ($\sim$51 keV of potential energy) was used to irradiate a 3 mm spot of clean float zone (FZ) silicon (100) (2X1) for a total dose of $\sim 5 \times 10^{11}$ ions. Due to the indirect nature of its band gap, bulk silicon is typically a poor photon emitter upon external excitation. However, as the crystal size approaches nanometer scales, the band gap widens due to quantum confinement and becomes direct allowing for more efficient photon emission. Ex-situ room temperature photoluminescence (PL) spectra were measured using a high resolution grating spectrometer with an excitation wavelength of 379 nm from a Titanium-Sapphire laser. PL spectra from areas exposed to SHCI bombardment show a broad emission centered at 504 nm. This is consistent with emission observed from 1-2 nm silicon nanocrystals. No PL is observed from similarly prepared FZ Silicon samples exposed to beams of 308 keV Xe^{27+} ($\sim$10 keV of potential energy) and 5 keV Xe^{1+} with comparable doses. A series of sharp lines at 548 nm, 534 nm, and 530 nm are also present in the PL spectrum from areas exposed to Xe^{44+} which is characteristic of an excitonic series in nanometer size direct band gap materials. The deposition of potential energy from Xe^{44+} produces a phase transition in silicon surfaces at nanometer size level that is not produced from normal singly charged ion bombardment. This work was performed under the auspices of the U.S. Department of Energy by Lawrence Livermore National Laboratory under contract No, W-74505-ENG-48.

SESSION T4:
Tuesday Morning, November 30, 1999
Room 310 (H)

8:30 AM *T4.1
STRUCTURE AND SPECTRAL PROPERTIES OF POINT DEFECTS IN SiO_2 AND Si_3N_4 FROM FIRST PRINCIPLE CALCULATIONS. Gianfranco Pacchioni, University of Milano-Bicocca, Dept. of Materials Science, Milano, ITALY.

The electronic structure and properties of point defects in dielectric materials, silicon oxide and nitride in particular, have been determined by means of ab initio methods and cluster models. Hartree-Fock, Density Functional Theory and Configuration Interaction calculations have been performed to determine the ground and excited state properties of the defects. In this way hyperfine coupling constants for paramagnetic defects, optical transitions, vibrational properties and NMR shieldings have been determined for a series of point defects. Special attention has been given to the charge conversion and charge transfer mechanisms and to the negative-U nature of some of the defects considered. The comparison between theory and experiment allows one to unambiguously assign the spectral features to a given defect structure and to compare the properties of structurally similar defects in silicon oxide and silicon nitride.

9:00 AM T4.2
BONDING ARRANGEMENTS AT THE Si–SiO_2 AND SiC–SiO_2 INTERFACES AND THE ORIGIN OF THEIR CONTRASTING PROPERTIES. Ryszard Buczko, Stephen J. Pennycook and Sokrates T. Pantelides, Solid State Division, Oak Ridge National Laboratory, Oak Ridge, TN; Department of Physics and Astronomy, Vanderbilt University, Nashville, TN.

The ultimate control of ultrathin gate in microelectronics and successful fabrication of SiC-based power MOSFETs hinge on understanding the factors that control the abruptness and smoothness of the Si–SiO_2 and SiC–SiO_2 interfaces. We present a systematic study of possible bonding at the interfaces. We raport ab initio calculations that are designed to explore the relative energetics of different structures. We find that the intrinisic geometry of the Si (001) surface and the softness of the Si–O–Si angle lead to totally abrupt (no suboxide layer) and smooth (no steps) Si–SiO_2 interface. However, two energetically degenerate phases are possible during growth at finit temperatures, leading to domain boundaries, that are the cause of suboxide bonds, steps, and dangling bonds. In principle, these effects may be avoidable by low-temperature deposition. In contrast, the geometry of SiC surfaces is not suitable for abrupt and smooth interfaces. In the Si–terminated cubic SiC (001) surface, all dangling bonds can be easly saturated by oxygen bridges terminating the growth of the silicon dioxide. The same total–saturation effect is favored by geometry in the (0001) surface of the hexagonal SiC. Careful examination of this surface revealed several other modes of total saturation, but no bonding arrangements that yield abrupt and smooth interfaces. Suboxide bonds seem inevitable.

9:15 AM T4.3
INITIAL NITRIDATION STEPS OF SILICON SURFACES INVESTIGATED BY COMPUTATIONAL CHEMISTRY. Seiichi Takami, Aruba Yamada, Akira Endou, Momoji Kubo, Akira Miyamoto, Tohoku Univ, Dept of Materials Chemistry, Sendai, JAPAN.

Electrical properties of dielectric films are susceptible to roughness of their interfaces as well as disorder of the films. A number of studies focused on the steepness of the interface between Si and SiO_2 layers as well as their electrical properties. Recently, the silicon oxinitride and silicon nitride films have been studied extensively as the perspective candidates for dielectric films. This study focused the initial course of nitridation of silicon surfaces using the computational techniques. Si(100) and (111) surfaces were represented by the top surfaces of model clusters, $Si_{60}H_{44}$ and $Si_{68}H_{46}$, respectively. In this

study, we investigated the energetic stability of nitrided clusters where a nitrogen atom bound with three silicon atoms at different sites. After the nitrogen atom was incorporated into the original cluster, the geometry of nitrided clusters were optimized and their enthalpy of formation was evaluated using a semiempirical AM1 hamiltonian function. We studied six possible structures that represent the nitridation of Si(100) surfaces and five of Si(111). The results indicate that the outermost silicon atoms on Si(111) surfaces were favorably nitrided as compared with the inner silicon atoms while significant differences were not observed on Si(100) between the top dimer site and the inner atoms. To account this tendency, the enthalpy of nitridation was divided to heat of deformation of Si lattice heat (ΔE_{def}) and heat of bond formation (ΔE_{bond}) between Si and N atoms. The heat of bond formation during nitridation on Si(111) is almost independent on nitridation sites. Therefore, differences in the enthalpy of nitridation between outer surface and inner atoms result from ΔE_{def}. On the other hand, there are no distinct relationship between the two energies, ΔE_{def} and ΔE_{bond} for Si(100). This leads to the absence of significant difference in the enthalpies of the nitridation of the Si(100) surfaces among various sites of nitridation.

9:30 AM T4.4
INITIAL OXYNITRIDATION OF Si(001)-2x1 SURFACE BY NITRIC OXIDE. Noriyuki Miyata, Heiji Watanabe, and Masakazu Ichikawa, Joint Research Center for Atom Technology, Angstrom Technology Partnership (JRCAT-ATP), Ibaraki, JAPAN.

A Si oxynitride layer thermally grown on a Si substrate is a leading candidate for the gate dielectric layer. Although the oxidation mechanism of the Si surface under pure oxygen has been well investigated by many researchers, few studies have dealt with the fundamental mechanism of oxynitridation. In this work, we report on the initial oxynitridation produced by nitric oxide (NO) on an atomically flat Si(001)-2x1 surface. The NO oxynitride layer was thermally grown on a clean Si(001)-2x1 surface under $2x10^{-6}$-$5x10^{-5}$ Torr NO pressure at 550-750°C. The atomic-scale structure at the oxynitride/Si interface was investigated by scanning reflection electron microscopy (SREM), and the chemical structure was investigated by XPS. For a first oxynitridation in which NO reacted with the first Si layer on the Si(001) surface, we observed that the terrace contrast in the SREM image was completely reversed. This result indicates that the first oxynitridation was caused by a layer-by-layer growth like an oxidation caused by oxygen.[1] However, for the further oxynitridation, the terrace contrast disappeared while the step contrast became apparent in the SREM image. A spot analysis of RHEED showed that the atomic-scale roughness at the oxynitride/Si interface increased with oxynitridation. These results indicate that the NO oxynitridation at the oxynitride/Si interface does not take place in a layer-by-layer fashion from the second Si layer. [This work is supported by NEDO.] [1] H. Watanabe, K. Kato, T. Uda, K. Fujita, M. Ichikawa, T. Kawamura, and K. Terakura, Phys. Rev. Lett. 80, 345 (1998).

9:45 AM T4.5
LOW TEMPERATURE OXIDATION OF SILICON(100) SUBSTRATES USING ATOMIC OXYGEN. Tomo Ueno, Shingo Chikamura, Fumito Sakuraba, Yoshitaka Iwasaki, Tokyo University of Agriculture and Technology, Faculty of Technology, Tokyo, JAPAN.

Low temperature oxidation process of Si(100) substrates using atomic oxygen has been proposed. For the generation of atomic oxygen, microwave plasma remotely attached on the oxidation chamber was used. In the microwave plasma, the large amount of rare gas and a small amount of O_2 gas mixture was supplied. The existence of the large amount of rare gas controls the plasma energy to some restricted values associated with the metastable states of the rare gas. Consequently, atomic oxygen were efficiently generated instead of excited O_2 molecules with any vibrational states. The oxidation kinetics of crystalline Si using this process was shown to be diffusion-limiting, even if the oxide thickness was less than several nm. The activation energy of B, which is referred to as the parabolic rate constant, was found to be 0.14eV. In addition, lower interface trap density of $2.6\times10^{11}/cm^2/eV$ at the mid gap could be achieved for the as-grown SiO_2/Si(100) interface at the processing temperature of 500°C.

10:30 AM T4.6
INTERFACIAL PROPERTIES OF ULTRA THIN SILICON DIOXIDE FILMS GROWN ON NITROGEN AND SILICON IMPLANTED SILICON. Michael Jackson, Nate Wescott, Santosh Kurinec, Microelectronic Engineering, Rochester Institute of Technology, Rochester, NY; Kent Zhuang and Gabriel Braunstein, Analytical Technology Division, Eastman Kodak Company, Rochester, NY.

It is well known that nitrogen implantation prior to oxidation severely retards oxidation rate in silicon. To determine, whether it is an implant damage related issue, silicon and diatomic nitrogen (amu is 28 for both) have been implanted with similar doses separately on different regions in the same Si wafer before oxidation. Oxidation kinetic studies reveal that silicon implantation has practically no effect on the initial growth rate of oxides on Si. The electrical nature of the thin oxide interface has been investigated by surface charge analyzer (SCA). The SCA works by forming a temporary gate contact, biasing the substrate from inversion to accumulation while stimulating the silicon surface via chopped light and recording and analyzing depletion region width as a function of polarity and magnitude of the induced charge. Quantities like the oxide charge at midgap Q_{ox}, oxide charge at flat band Q_{FB}, interface trap density D_{it}, and minority carrier lifetime, have been obtained from this data. The lifetime extraction is done from data relating induced charge to modulated light intensity under inversion. The software allows plotting wafer maps of these quantities, which show a distinct change in Q_{FB}, D_{it}, and lifetime in the regions corresponding to Si and N_2 implants. At a dose of $4\times10^{14}/cm^2$ and above, N_2 implantation in Si prior to oxidation increased the Q_{ox}, D_{it}, and lifetime considerably compared to equivalent Si implantation. The structure of the Si-SiO_2 interface has been probed using angle resolved X-ray photoelectron spectroscopy that gives the depth profiles for Si, O, and N without causing the damage due to ion gun sputtering employed in conventional XPS and SIMS. The results show that the interface is less abrupt in the case of nitrogen-implanted silicon, indicating the presence of a reduced sub oxide density at the interface. These studies suggest that the interfacial properties are primarily governed by the chemical presence of nitrogen rather than the damage caused by implantation.

10:45 AM *T4.7
DEFECT STUDIES IN NITRIDED Si/SiO_2 STRUCTURES. J.L. Cantin, H.J. Von Bardeleben, Groupe de Physique des Solides, Universités Paris 6&7 et CNRS, FRANCE.

The modification of the ultra thin SiO_2 layers by nitridation has found an increasing attention in the last years as it has been shown to produce an efficient barrier for boron diffusion from the polysilicon top layer of modern transistors, without degrading the quality of the dielectric [1,2]. Various sequences of nitridation and re-oxidation steps have been attempted to optimise ultra thin oxynitrides layers in terms of electrical performance and processing conditions [4]. Essentially, rapid thermal or furnace annealing in NH_3, NO_2 and NO atmospheres were explored. We have recently shown that, in addition, a strong reduction of interface defect concentration can be obtained in certain cases [3]. We will focus on the modification of the Si/SiO_2 interface structure after annealing in the 950°C temperature range, in NO to avoid the complications induced by the decomposition of NH_3 and N_2O molecules. We analyzed the nitridation effect on the interface structure by electron paramagnetic resonance using the intrinsic defect of this interface, P_{b0} and P_{b1} as local probes. The same layers were equally analyzed by nuclear reaction analysis which allows to determine the total nitrogen content and its localisation [5]. Combined monitoring of the interfacial defect concentration at each nitridation step, allows us to propose different reaction mechanisms for the nitrogen incorporation in the dielectric and at the interface.
References:
[1] The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface 3', H.Z. Massoud, E.H. Poindexter, C.R. Helms (Eds.), The Electrochemical Society Inc., (1996)
[2] Z.Q. Yao et al., IEEE Elec. Dev. Lett. 15, 516 (1998)
[3] L.G. Gosset et al, J. of Appl.Phys. 85, 3661 (1999)
[4] H.C. Lu, Microelectronic Engineering 36, 29 (1997)
[5] L.G. Gosset et al., NIM B 136-138, 521 (1998)

11:15 AM T4.8
THEORETICAL AND EXPERIMENTAL INVESTIGATION OF ULTRA-THIN OXYNITRIDES. A. Demkov and R. Liu, Semiconductor Products Sector, Motorola, Inc., Mesa, AZ.

Silicon Oxynitrides SiO_xN_y are important in many applications in the semiconductor industry. Most often they are observed in the interfacial regions e.g. between the oxide and the nitride. The properties of these thin layers are not yet well understood, and even the very thermodynamic stability of the material is questioned. Perhaps, some of the most important questions are the nitrogen distribution at the interface, and the effect of nitrogen on the atomic structure and ultimately on the transport properties such as a band offset and electron mobility. To achieve a better understanding of these effects we use a combination of the infra-red ATR and ab-initio electronic structure methods. We use a theoretical structural model model of the $SiSiO_2$ interface with the oxide thickness of 0.8 nm. The interfacial region amounts to about 0.4 nm (the total thickness of the oxygen containing layer is 1.2 nm). The Density Functional Quantum Molecular Dynamics simulations suggest that N accumulates at the interface. The physical reason for this is the chemical nature of nitrogen. Nitrogen prefers a three-fold coordinated structure, which is

impossible to realize within the oxide layer without the introduction of defects. We have generated samples with the nitrogen concentrations from 1.69 x 10^{14} cm^{-2} to 6.78 x 10^{14} cm^{-2}. The structural analysis of the nitrogen containing structure indicates a significant improvement of the oxide layer and the interface. We have performed a calculation of the vibrational density of states. A N-localized mode at 809 cm^{-1} has been identified. The experimental ifnra-red ATR data is in qualitative agreement with the calculation. The valence band offset calculations revealed a 0.3 eV increase of the offset due to nitrogen at the highest nitrogen concentration considered. As a result a 0.8 nm oxynitride is equivalent to a 1.2 nm pure oxide. The valence band offset increase comes mainly from the structural change in the oxide layer. The interfacial dipole contributes 0.12 eV to the increase, while the structural change in the oxide layer gives additional 0.2 eV. The increase of the valence band offset may indicate the decrease of the conduction band offset, which will result in a higher leakage current of the electron device; there could, however, be an improvement for hole devices.

11:30 AM T4.9
PARAMAGNETIC DEFECTS RELATED TO POSITIVE CHARGES IN SILICON OXYNITRIDE FILMS. Y. Miura, and S. Fujieda, NEC Corporation, Silicon Systems Research Laboratories, Tsukuba, JAPAN; E. Hasegawa, NEC Corporation, ULSI Device Development Laboratories, Sagamihara, JAPAN.

Nitrogen incorporation into gate oxides substantially improves MOS device reliability. However, positive charge generation in oxynitride films has been reported to decrease channel mobility. We have examined a new type of paramagnetic center specific to silicon oxynitrides. To investigate the relationship between the positive charge center and the paramagnetic center, we compared the densities of both centers and the changes in the densities induced by vacuum ultraviolet (VUV) irradiation and hydrogen annealing (400°C. Oxynitride films with thicknesses of 6-10 nm were grown on Si(100) p-type wafers in a N_2O ambient within a furnace. The spin densities of the paramagnetic centers and the positive charges were determined by electron spin resonance (ESR) and C-V (100 kHz) measurements. The as-grown oxynitrides showed an ESR signal (g=2.0006). This g value suggests that the paramagnetic centers are a kind of Si dangling bond (an E_γ' center). However, the saturation characteristics differed from those of stress-induced E_γ' centers. The spin density was comparable with half of the charge density. Since the spin density increases with the nitrogen concentration, we inferred that the paramagnetic centers in oxynitrides (the E_γ'-like centers) are produced by the N incorporation process. The charges and spins were almost completely eliminated after VUV irradiation, but were not affected by hydrogen annealing. Based on the similar behaviors of the positive charges and the E_γ'-like centers, we conclude that a significant number of the positive charges are originated from Si bonding defects.

11:45 AM T4.10
FURNACE OXYNITRIDATION IN NITRIC OXIDE OF THIN SILICON OXIDES: ATOMIC TRANSPORT MECHANISMS AND INTERFACIAL MICROSTRUCTURE. Isabelle Trimaille, Jean-Jacques Ganem, Laurent G. Gosset, Olivier Bailly, Serge Rigo, Jean-Louis Cantin, Hans Jurgen von Bardeleben, Universities Paris 7 and Paris 6, Groupe de Physique des Solides, UMR-CNRS 75-88, Paris, FRANCE.

Oxynitridation in nitric oxide of commercial 5 nm and 13 nm oxides is investigated, as well as reoxidation steps. The use of the thicker film has a twofold justification :i) the decorrelation of surface reactions (exchange of atoms between the gas phase and the film) from interfaces reactions (incorporation in the film of atoms from the gas phase) ; ii) the comparison of atomic transport mechanisms occurring in furnace oxynitridation (this work) with those observed in RTP oxynitridation, which was the issue of a previous work. We performed on the oxide films isotopic sequential thermal treatments : $^{14}N^{16}O/^{18}O_2$ and $^{15}N^{18}O/^{16}O_2$. The atomic areal densities (^{14}N,^{15}N,^{16}O,^{18}O) in the films were measured using nuclear reactions analysis, with a sensitivity between 0.01 to 0.15 monolayer, depending on the isotopic species. The concentration depth profiles of the heavy and stable isotopes (^{15}N,^{18}O) were determined with near surface depth resolution of 0.5 and 0.7 nm respectively using narrow, low energy nuclear reactions resonances. The results are discussed in terms of atomic transport mechanisms and modification of interfacial microstructure. The most striking result is that during reoxidation steps neither loss or observable redistribution of nitrogen is evidenced, which is not the case when direct oxynitridation in nitric oxide or in nitrous oxide is performed on silicon. Reoxidation delay is commonly used as an assessment of the nitrogen content of the film. Thanks to isotopic tracing, we measure only oxygen atoms incorporated in the film during the reoxidation step, allowing a precise quantification of reoxidation. To scan the evolution of the interfacial microstructure, Pb centers concentrations were measured by paramagnetic electron resonance spectroscopy, after each thermal treatment step.

SESSION T5:
Tuesday Afternoon, November 30, 1999
Room 310 (H)

1:30 PM *T5.1
CHALLENGES IN INTERFACE TRAP CHARACTERIZATION OF DEEP SUB-MICRON MOS DEVICES USING CHARGE PUMPING TECHNIQUES. Jean-Luc Autran, Pascal Masson, LPM, INSA de Lyon, FRANCE; Gèrard Ghibaudo, LPCS, ENSERG, Grenoble, FRANCE.

With the ever shrinking of device dimensions, deep sub-micron MOS transistors enter now in a critical range where quantum-confined effects, tunneling leakage mechanisms and single-trap activity make their characterization more and more difficult from the electrical point-of-view. This is particularly true for the characterization of the $Si\text{-}SiO_2$ interface in such ultra-thin MOS systems which requires the development of new experimental approaches to correctly probe interface and near-interface traps. The aim of this contribution is to review the latest experimental and theoretical developments concerning the charge pumping techniques, recognized from the two last decades as powerful tools for the characterization of dielectric-silicon interfaces in a wide variety of advanced devices. This family of techniques is based on the exploitation of a repetitive process whereby majority carriers coming from the substrate recombine with minority carriers previously trapped in interface states, when the MOS transistor is submitted to well-chosen biasing cycles. By taking into account the emission processes which control the exchange of charges at the interface, interface trap characteristics such as the density and the capture cross sections for electrons and holes can be obtained. This survey will particularly focus on the way to adapt charge pumping techniques and extraction models in the case of ultra-thin oxides or non-planar interfaces. Extended results concerning the electrical activity of the $Si\text{-}SiO_2$ interface, deduced from these techniques, will be reported. Finally, we will present a new modeling of the charge-pumping phenomenon based on an improved time domain analysis considering the time- and energy-resolved evolutions of the trap filling probability in the semiconductor bandgap. The case of the single-trap modeling will be also treated.

2:00 PM T5.2
PHOTOLUMINESCENCE CHARACTERIZATION OF DEFECTS IN THERMAL OXIDE. Hiroyuki Nishikawa, Tokyo Metropolitan Univ., Dept. of Electrical Engineering, Tokyo, JAPAN; James H. Stathis, IBM T. J. Watson Research Center, NY.

In recent years, identification of defects in thermal oxides has become one of the most important issues to assure high-quality ultra-thin gate oxide for the MOS structures in rapidly down-scaling LSI devices. While the electron-spin-resonance (ESR) technique is restricted to characterization of paramagnetic defects, optical spectroscopy such as a photoluminescence (PL) technique has a potential to provide more useful information on defects in thermal oxide. Samples are thermal oxides with thicknesses of 29-45 nm grown at 850-1000°C in dry oxygen on Si(111) or (100) substrate. Some were annealed in forming gas and were subsequently either annealed in vacuum ($<10^{-7}$ Torr) at 700°C for 2 hours, or exposed to atomic hydrogen. The PL measurements were carried out at room temperature using a fluorescence spectrometer installed at the beamline U9B in the National Synchrotron Light Source facility (Brookhaven National Laboratory, New York) under excitation from the SR light. A 3.3 eV PL was observed for the passivated oxide on Si (111) substrate after the forming-gas anneal. Similar PL band was also observed for oxynitride film. The dehydrogenation by the vacuum annealing generates increased PL intensity by a factor of about 1.5, revealing the latent PL centers in the passivated thermal oxide, while the exposure to atomic hydrogen almost passivates the PL active centers. Therefore, the activation and deactivation of the 3.3 eV PL centers can be explained by the reaction of the PL centers with atomic hydrogen. Possible origin of the PL centers will be discussed in comparison with defects such as P_b and EX centers detected by ESR reported for thermal oxide.

2:15 PM T5.3
INTERFACE CHEMISTRY OF GATE DIELECTRICS ON SILICON. E. Garfunkel, H.C. Lu, W.H. Schulte, N. Yasuda, T. Gustafsson, Departments of Chemistry and Physics, and Laboratory for Surface Modification, Rutgers University, Piscataway, NJ; G. Alers and M. Green, Lucent Technologies-Bell Laboratories, Murray Hill, NJ.

New insights into future generation gate dielectrics, including both silicon nitride and high-k metal oxides, is coming from several sources including ion beam analysis. In this paper we present new ion beam and surface analytical results on the structure and chemistry of novel layered gate dielectric structures, especially at the interfaces between materials. Experimental methods to be discussed include medium energy ion scattering, Rutherford backscattering spectroscopy, nuclear

reaction analysis and profiling, photoemission and scanning probe microscopy. Materials being explored include combinations of stable and meta-stable metal oxides on silicon. We discuss both conventional and novel routes to making these higher-k dielectrics that will allow them to be incorporated in MOS structures such that the total effective gate oxide thickness will be under 1 nm. Electrical measurements and their interpretation will also be briefly presented.

2:30 PM *T5.4
SINGLE-EVENT GATE RUPTURE IN THIN GATE OXIDES. A NEW TERRESTRIAL COSMIC-RAY VULNERABILITY?
Fred Sexton, Sandia National Laboratory, Albuquerque, NM.

Single event gate rupture (SEGR) is a catastrophic failure mode that occurs in dielectric materials that are struck by energetic heavy ions while biased under a high electric field condition. SEGR can reduce the critical electric field to breakdown to less than half the value observed in normal voltage ramp reliability tests. As electric fields in gate oxides increase to greater than 5 MV/cm in advanced MOS technologies the impact of SEGR on the reliability of space based electronics must be assessed. Recent work has shown that the critical field to rupture increases with decreasing oxide thickness, and is correlated with the increasing dielectric strength of thin oxides. The observed dependence of inverse critical field to rupture on ion linear energy transfer (LET) and bias voltage has been described in terms of a physical model of the conductive path for discharge through the oxide. This model relates the resistance of the conductive "pipe" through the oxide to the density of electrons injected from two sources: 1) those due to an applied voltage and 2) those due to energy deposition along the path of the heavy ion. The observed angular dependence of SEGR in thin oxides is well described by this model. This work also shows that SEGR is a true single ion effect and that the buildup of damage from high fluences of ions at biases below critical voltage to rupture, VCR, does not affect breakdown. Also, the incorporation of nitrogen near the oxide-silicon interface, which increases the resistance to charge trapping and the subsequent reliability of thin oxides, does not affect SEGR.
In this summary, we explore the nature of SEGR in oxides with thickness from 7 nm to less than 5 nm, where soft breakdown is often observed during traditional reliability tests. We discuss the possible connection between the present understanding of SEGR and voltage stress breakdown models. Recent work showing a dependence of SEGR on ion atomic number rather than ion LET is also discussed.

3:30 PM *T5.5
THE IMPACT OF TEMPERATURE AND BREAKDOWN STATISTICS ON RELIABILITY PREDICTIONS FOR ULTRA-THIN OXIDES. G. Groeseneken, R. Degraeve, B. Kaczer, H.E. Maes, IMEC, Leuven, BELGIUM.

In this paper, the reliability of ultra-thin oxides for the Giga-scale technologies will be discussed. It will first be demonstrated that with the decreasing oxide thickness the statistical spread of time-to-breakdown increases. This is due to the nature of the intrinsic breakdown mechanism, which is associated with the formation of a percolation path through the randomly generated neutral electron traps in the oxide. This larger statistical spread has important consequences for both the low percentile and the area scalings of time-to-breakdown. Consequently, the area and the percentile should always be indicated in any reliability specification. It will also be demonstrated that due to the transition from Fowler-Nordheim tunneling to direct tunneling and the occurrence of ballistic transport in the oxide, constant current stress becomes meaningless, and the time-to-breakdown correlates better with the applied voltage. It will be shown that the frequently reported polarity gap in charge-to-breakdown is an artifact of the constant current method and disappears when constant voltage is applied.
With the operating temperature of logic integrated circuits likely to rise to the 100 150 C range for the upcoming technology generations, the issue of temperature acceleration of time-to-breakdown of gate SiO_2 films becomes significant. We will therefore also present a study of the effect of elevated temperature on the gate oxide breakdown. A strongly increasing temperature dependence of the breakdown is observed for decreasing oxide thickness. We also find that the Arrhenius law does not describe the process well, in contrast to that we find that the log of time-to-breakdown appears to scale linearly with temperature for a wide range of oxide thicknesses. We further observe that the density of neutral traps at breakdown also decreases with increasing temperature. Possible explanations for these phenomena will be proposed.
All this means that one should be careful when using the charge-to-breakdown value obtained on a test capacitor as the only figure-of-merit for the oxide reliability, as was often done in the past. The combined effect of the increased statistical spread, the percentile and area scalings and the increased temperature dependence leads to strongly reduced reliability margins for ultra-thin SiO_2. Our predictions indicate that reliability might become a showstopper for further oxide scaling necessary for Giga-scale technologies, emphasising the need for alternative dielectrics earlier than was forecasted before, based on leakage current only.

4:00 PM *T5.6
RELIABILITY OF ULTRATHIN GATE OXIDES. D.J. DiMaria and J.H. Stathis, IBM Research, Yorktown Heights, NY.

Aggressive scaling of the oxide thickness for future MOS logic and memory technology requires, among other concerns, an assurance that the oxide can meet requirements for reliability. Defects generated by electrons tunneling through the gate oxide ultimately lead to destructive breakdown. In this work we have investigated the relationship between the rate of defect generation and the gate voltage down to voltages where transport occurs by direct tunneling. Next, the critical defect density at breakdown has been measured as a function of oxide thickness in the range 1.4 to 5.0 nm. The complete thickness dependence is well described by a percolation model. Finally, the breakdown statistics appropriate for thin oxides are used to predict time-to-breakdown at low voltage for chips built with ultra thin gate oxide. Our model predicts that oxide reliability will limit the oxide scaling to about 2.6 nm (CV extrapolated thickness) or 2.2 nm (QM thickness) for a 1V supply voltage and that the current Semiconductor Industry Association (SIA) roadmap will be unattainable for reliability reasons by sometime early next century.

4:30 PM T5.7
ELECTRICAL AND PHYSICAL CHARACTERIZATION OF ULTRATHIN SILICON OXYNITRIDE GATE DIELECTRIC FILMS FORMED BY THE JET VAPOR DEPOSITION TECHNIQUE.
A. Karamcheti, V.H.C. Watt, T.Y. Luo, D. Brady, F. Shaapur, L. Vishnubhotla, G. Gale, H.R. Huff, M.D. Jackson, K. Torres, A. Diebold, J. Guan, M.C. Gilmer, G.A. Brown, G. Bersuker, P. Zeitzoff, SEMATECH, Inc., Austin, TX; T. Tamagawa, Jet Process Corporation, New Haven, CT; X. Guo, X.W. Wang and T.P. Ma, Dept. of Electrical Engineering, Yale University, New Haven, CT.

This paper describes the electrical and physical characteristics of ultrathin Jet Vapor Deposited (JVD) Silicon Oxynitride films. Capacitance-Voltage measurements indicate an equivalent oxide thickness of less than 2 nm (less than 2.5 nm without quantum-mechanical and poly-depletion corrections). These films have leakage currents almost two orders of magnitude lower than thermal oxide of the same equivalent thickness. Fowler-Nordheim tunneling is seen to be the dominant conduction mechanism. Measurements on NMOSFETs with 0.15 μm of channel length demonstrate excellent electrical properties, including high drive currents ($\sim$0.5 mA/μm @ V_d=V_g-V_t=1.5 V), low sub-threshold swings ($\sim$72 mV/decade), and high transconductance ($\sim$0.36 mS/μm @ V_d=1.5 V). These films were also analyzed using a variety of physico-chemical methods, including Total X-ray Fluorescence (TXRF), Atomic Force Microscopy (AFM), Low Energy (500 eV) Secondary Ion Mass Spectroscopy (SIMS), Transmission Electron Microscopy (TEM), Medium Energy Ion Spectroscopy (MEIS), Fourier Transform Infrared (FTIR) spectroscopy, and Nuclear Reaction Analysis (NRA). TXRF measurements on the JVD films indicate a surface metal concentration $\sim 5 \times 10^{10}$ atoms/cm^2 - 1×10^{11} atoms/cm^2. Micro-roughness analysis performed by AFM show the films to be very smooth - RMS values varied between 0.1 - 0.2 nm. SIMS (500 eV) and NRA indicate high [N] near the top as well as throughout the bulk of the film, and a significant amount of [O] in the bulk as well as near the Si/Oxynitride interface. High Resolution TEM pictures show a very uniform film with a physical thickness of 2.8 $\pm$ 0.3 nm which, when converted to T_{ox}, validates the equivalent thickness measured electrically, for these types of oxynitride films.

4:45 PM T5.8
INTEGRATION OF INDEPENDENT TUNNELING REDUCTIONS FROM i) NITRIDED INTERFACES AND ii) STACKED OXIDE NITRIDE GATE DIELECTRICS TO ACHIEVE COMBINED REDUCTIONS IN DIRECT TUNNELING WITH RESPECT TO OXIDE GATE DIELECTRICS OF >200 FOR pMOS AND nMOS DEVICES WITH OXIDE-EQUIVALENT THICKNESS TO 1.3 nm.
G. Lucovsky, Yider Wu, Yi-Mu Lee, and Hiro Niimi, NC State Univ, Raleigh, NC.

Two independent mechanisms for tunnel current reduction, i) interface nitridation and ii) replacement of oxides by physically-ticker nitrides have been combined initially in stacked 'NON' dielectrics to yield current densities $<10^{-2}$ A/cm^2 for an oxide-equivalent thickness (tox-eq) $\sim$1.6 nm, and $<$1 A/cm^2 for tox-eq $\sim$1.3 nm. Stack fabrication combines remote plasma-assisted oxidation, nitridation and deposition processes to independently control N-profiles/concentrations i)at the monolayer level at the Si-SiO$-$2 interface and ii)in the bulk nitride film. The processing order of interface nitridation is crucial and the monolayer concentrations required to reduce direct tunneling by $\sim$10 utilize two steps i) remote

plasma-assisted oxidation of H-terminated Si(100) to form an ~0.6 nm passivating oxide, followed by ii) remote plasma-assisted nitridation to insert approximately one monolayer of N-atoms at the Si-interface. Integration of nitrides into 'NON' stacks provides physically thicker films while maintaining capacitance equivalent to thinner oxides; however, for these plasma-deposited nitrides, increases in thickness alone (as in 'ON' stacks) are in part compensated by decreases in the product of the tunneling mass and thickness-averaged-barrier-height, thereby limiting tunneling reductions with respect to oxides in devices without intentional interface nitridation to ~10-20 for tox-eq ~1-5 to 2 nm. However, it has been possible to combine the independent interface and bulk thickness current reduction effects in 'NON' stacks, and in this way achieve reductions in tunneling relative to oxides exceeding 200. These stacks have been integrated into nMOS and pMOS FETs which display high current drive with <5% reductions in peak channel mobility. Decreases in transconductance are typically <2% after accelerated stressing at average fields >15 MV/cm and at integrated doses exceeding 10^4 C/cm^2. Supported by NSF, SRC, and ONR.

SESSION T6:
Wednesday Morning, December 1, 1999
Room 310 (H)

8:30 AM *T6.1
THE BOUNDARY BETWEEN HARD AND SOFT BREAKDOWN IN ULTRA-THIN SLICON DIOXIDE FILMS. Akira Toriumi, Hideki Satake, Toshiba Corporation, Advanced LSI Technology Laboratory, Kawasaki, JAPAN.

We have noticed that the post-breakdown electrical properties of silicon dioxide films include a number of information on the dielectric breakdown mechanism. And the discharging energy at the breakdown has been introduced to describe the resistance of silicon dioxide films after the hard breakdown in relatively thicker oxides [1], where it is defined as the difference of the energy stored in the capacitor between the pre- and post-breakdown. On the other hand, the breakdown mechanism becomes the soft-breakdown in the ultra-thin silicon dioxides from the hard breakdown in thicker oxides. In this paper, we report further study of the post breakdown analysis of silicon dioxide films to discuss that the boundary between the soft and the hard breakdown is critically dependent on the discharging time constant as well as the discharging energy at the breakdown. In particular, it is worthwhile to pay attention to the fact that the ratio of the soft to the hard breakdown changes in terms of the statistical distribution, by changing the parameters in the growth and the measurement conditions. This fact will be essentially important to assess the silicon dioxide reliability in sub-5nm regime. [1] H. Satake and A. Toriumi, Tech. Dig. VLSI Symp. (1999), p. 61, (Kyoto).

9:00 AM T6.2
A STUDY OF TRAP PROFILES IN THIN SILICON DIOXIDE FILMS AT DIELECTRIC BREAKDOWN USING PERCOLATION MODEL. Shigeyasu Uno, Akihiro Ishida, Kenji Okada, Toshiki Sakura, Kazuaki Deguchi, Yoshinari Kamakura, Kenji Taniguchi, Osaka Univ, Dept of Electronics and Information Engineering, Osaka, JAPAN.

We have studied the electron trap distributions at dielectric breakdown in thin gate oxide films. Through the study, we introduced a percolation model with non-uniformity of trap generation. As a result, we convince that the exponential distribution decaying from Si/SiO_2 interface is the most appropriate to explain the electrical characteristics of MOSFETs just before the breakdown. We measured electron charge centroid as well as Vt shifts at breakdown, which depends on stress biases and carrier injection methods, for n-channel MOSFETs with oxide thickness of 7 nm. In order to connect these two quantities consistently, a computer simulation with a percolation concept was carried out. This model generates electron traps with a given generation probability as a function of depth from Si/SiO_2 interface based on the charge centroid information given by experiment. It can simulate Vt shifts at breakdown, and we found that the model with exponential trap distribution gives the most precise reproduction of Vt shifts for the gate voltages ranging from 6.5 to 9.1 V. Good agreements between experiment and simulation strongly supports the idea that traps are exponentially generated in the oxide layer. This result can be an important information for studies on dielectric breakdown phenomena in MOSFETs, and accelerates understanding of it.

9:15 AM T6.3
MEASUREMENT TECHNIQUE, OXIDE THICKNESS AND AREA DEPENDENCE OF SOFT-BREAKDOWN. Tanya Nigam, Bell-Labs, Lucent Technologies, Murray Hill, NJ; R. Degraeve, G. Groeseneken, M.M. Heyns, and H.E. Maes, IMEC, Leuven, BELGIUM.

For sub-5 nm oxides there are two different stages for breakdown; soft breakdown (SBD) and hard breakdown (HBD). It has been shown that both SBD and HBD exhibit the same statistics [1]. Therefore, the physical mechanism governing them is the same. The major difference between them is the energy transferred from the capacitor to the localized conducting path. In this paper, a simple equivalent circuit is proposed to explain the effect of the measurement technique, oxide thickness, and test structure area on the detection of soft breakdown. Also an inelastic quantum tunneling model is proposed to discuss the current-voltage characteristics after SBD.

Equivalent Circuit

For constant current stress (CCS), a decrease in applied voltage (V_{INT}) is measured after SBD. This leads to the discharge of the capacitor through the localized conducting path. The energy released through the breakdown path is given by

$$\Delta E = C(V_{INT}^2 - V_{SBD}^2)/2 = \frac{CV_{INT}^2}{2}\left[1 - \left(\frac{R_{SBD}}{R_{tun}}\right)^2\right]$$

Using the equations for CCS and constant voltage stress (CVS) it will be shown that: (i) Decreasing oxide thickness leads to an increase in SBD events for both CCS and CVS. (ii) For a fixed oxide thickness, decreasing the applied gate voltage and the test structure area leads to an increase in SBD events. (iii) For both CCS and CVS, decreasing the test structure area makes it easier to detect soft breakdown. (iv) For CVS, after SBD the increase in gate current is independent of area, confirming that SBD is a localized phenomenon.

Inelastic quantum tunneling Model

The current-voltage (IV) characteristics after SBD exhibit a power law dependence. In this work, for the first time, it will be shown that the slope of IV characteristics exhibits quantization. This phenomena can not be explained by any of the existing models. Using inelastic quantum tunneling model the quantization in the slope will be explained by the change in number of traps participating in the current conduction. The model is also successful in explaining the temperature dependence of SBD IV characteristics.
The models and the experimental results will be presented at the conference.

Reference

(1) E. Wu, E. Nowak, J. Aitken, W. Abadeer, L.K. Han, and S. Lo, IEDM Tech. Digest, pp.187-190(1998).

9:30 AM T6.4
EXPERIMENTAL AND THEORETICAL STUDY OF STRESS-INDUCED LEAKAGE CURRENT IN THIN OXIDES STRESSED BY CORONA CHARGING IN AIR : RELATIONSHIP TO GOI DEFECTS. Marshall Wilson, Jacek Lagowski, Alexandre Savtchouk and Dmitriy Marinskiy, Semiconductor Diagnostics, Tampa, FL Lubek Jastrzebski and John D'Amico, Center for Microelectronics Research, University of South Florida, Tampa, FL.

It has been recently shown that corona charging in air combined with non-contact oxide charge measurement with a CPD (contact potential difference) probe provides a new possibility for fast monitoring of I-V characteristics without preparation of MOS capacitors. Furthermore, it has been found that corona charging of thin oxides above the tunneling threshold is very effective in generating stress-induced leakage current (SILC). In this work we demonstrate the remarkable sensitivity of the corona SILC magnitude to GOI defect density. The experimental results cover three of the most common GOI defects, namely: 1 - the defects induced by heavy metals (Fe,Cu) at a practically important low concentration range of 1E10 to 1E11 atoms/cm^3; 2 - the defects originating from interface roughness and 3 - the defects related to crystal originated particles (COP). At low corona stress fluence, these defects play no role in the I-V characteristics which follow ideal Fowler-Nordheim plus Direct Tunneling current characteristics with a relative contribution from each process determined by the oxide thickness. At high corona stress fluences, GOI defects greatly increase the magnitude of SILC measured at a constant oxide field. This SILC current is analyzed in terms of an inelastic tunneling model involving stress-induced traps. It is suggested that the GOI role is associated with the enhanced rate of the trap generation during stress. Direct measurement of interface trap density and flat band voltage shift support this SILC mechanism. It is noted that the present findings employ a highly advantageous, novel methodology for GOI monitoring based on corona charging and CPD measurement.

10:15 AM *T6.5
A NEW TYPE OF SUPERLATTICE : AN EPITAXIAL SEMICONDUCTOR-ATOMIC SUPERLATTICE, SAS. Raphael Tsu, UNC-Charlotte, Charlotte, NC.

Conventional superlattices consist of alternating epitaxial layers of lattice matched or nearly matched strain-layers. Most systems involve III-V and II-VI compound semiconductors. For silicon, strain-layer superlattice of Si-Ge system results in quantum confinement in the

germanium layer apart from the fact that the barrier height is rather small. Several years ago, a new type of semiconductor superlattice, with adsorbed oxygen between adjacent silicon layers, shows continuation of epitaxy. Silicon grown beyond the Si/O barrier region is epitaxial with defect density below 1E9/cm^2. We have grown up to 9 periods of Si/O- and Si/CO-Superlattices showing electroluminescence in the visible spectrum without degradation operated continuously for more than one year. The hybridized orbitals dominate in both SAS and ALE, atomic layer epitaxy. However in SAS, the structure beyond the first couple of monolayers is overwhelmingly dominated by the silicon bonding configuration, i.e. the Si/O- as well as the Si/CO-Superlattice is basically silicon, which is compatible with silicon processing technology. Therefore, SAS may serve as silicon based LEDs and SOI for electronic and optoelectronic devices.

10:45 AM T6.6
Si/SiO_2 INTERFACE DEFECTS IN Si NANOCRYSTALS. G. Allan, C. Delerue, IEMN, Dept ISEN, Lille, FRANCE; M.V. Wolkin, P.M. Fauchet, Dept of Electrical and Computer Engineering, University of Rochester, NY.

The study of silicon quantum dots is a very active field of research because of promising applications in advanced electronic and optoelectronic devices. The quality of the interface between the silicon core and the oxide layer formed at the surface has a large influence on the electrical and optical properties of the dots. In the case of small dots (e.g. diameter $< \sim$3nm), defect states may appear in the band gap due to its opening induced by the strong confinement. Recently, we have shown that there is a substantial red shift in the luminescence of Si crystallites initially passivated by hydrogen when they are exposed to air or oxygen (M.V. Wolkin et al., Phys.Rev.Lett. 82, 197 (1999)). This has been interpreted as the presence of localized levels in the band gap of nanocrystals induced by oxygen. The goal of this paper is to present ab initio and semi-empirical electronic structure calculations for various situations involving oxygen atoms at the surface of Si clusters. We obtain that normal Si-O-Si and Si-O-H bonds do not give localized gap states. Similar results are obtained for Si-O-O-Si bonds. In contrast, we show that Si=O bonds give rise to deep states for dots smaller than $\sim$3 nm which could well explain the red shift of the luminescence. Other situations are presently investigated with more complex geometries. The influence of the stresses that occur at the $Si\text{-}SiO_2$ interface and are likely to play an important role in this problem is analyzed.

11:00 AM T6.7
OPTICAL CHARACTERIZATION OF QUANTUM-CONFINED Si/SiO_2 STRUCTURES. Y. Kanemitsu, Graduate School of Materials Science, Nara Institute of Science and Technology, Takayama, Ikoma, Nara, JAPAN.

The goal of achieving efficient luminescence in Si materials has stimulated considerable research in understanding electronic band structures of Si nanostructures. Indirect gap bulk semiconductors like crystalline Si (c-Si) do not show efficient light emission at room temperature. However, visible luminescence from Si nanocrystals has been observed at room temperature. It is expected that the relaxation of the k-selection rules due to confinement and structural disorder will lead to drastic modification of optical responses of Si materials. We have prepared amorphous Si (a-Si) and crystalline Si (c-Si) based quantum wells (QWs) and dots (QDs) and studied their electronic structures by means of resonant excitation spectroscopy. Zero-dimensional a-Si/SiO_2 and c-Si/SiO_2 QDs and two-dimensional a-Si/SiO_2 and c-Si/SiO_2 QWs show broad luminescence in the red spectral region even at room temperature. Under resonant excitation at energies within the PL band, the TO-phonon related structure is clearly observed in large c-Si/SiO_2 QDs and c-Si/SiO_2 QWs. The momentum-conserving-TO-phonon-assisted PL spectra show that the interior delocalized state exhibits the indirect-gap semiconductor nature like bulk Si and visible PL comes from the interior states. However, in very small c-Si/SiO_2 QDs, fine structures due to the Si-O-Si vibrations ($\sim$1100 cm^{-1}) are observed in the resonant PL spectrum. These vibrational structures in c-Si/SiO_2 QDs are similar to those of a-Si/SiO_2 QDs. The Si-O-Si vibration-modified structure in the PL spectra suggests that excitons and carriers are localized at the Si/SiO_2 interface in very small nanostructures. The understanding of electronic structures of quantum-confined c-Si/SiO_2 systems is an inevitable step toward realization of high-performance nanoscale semiconductor devices.

11:15 AM T6.8
QUANTUM CONFINEMENT IN NANOCRYSTALLINE Si SUPERLATTICES. G.F. Grom, P.M. Fauchet and L. Tsybeskov, Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY; J.P. McCaffrey, J.-M. Baribeu and D.J. Lockwood, Institute for Microstructural Sciences, National Research Council, Ottawa, CANADA.

Several spectroscopic techniques including photoluminescence (PL) and differential conductance were used to probe the effect of quantum confinement in nanocrystalline silicon (nc-Si)/SiO_2 superlattices (SLs). The nc-Si/SiO_2 SL is a layered structure consisting of nanometer-size Si nanocrystals (diameter from 15 to 4 nm with a size distribution of $\leq$ 5%) separated by ultra-thin SiO_2 layers (10-30 $\AA$). The structure in the PL spectra reveals the coexistence of phonon-assisted and direct, no-phonon electron-hole recombination in the Si nanocrystals. In accordance to the model of carrier confinement, a blue shift up to 0.4 eV is observed in the PL spectra of small Si nanocrystals. This result is consistent with the photocapacitance spectroscopy data: our measurements indicate a strong bandgap opening in $<$ 5 nm Si nanocrystals. The effect of hole confinement in the nc-Si SL has been studied using tunnel conductance spectroscopy. The measurements reveal a rich structure attributed to the resonant tunneling. Similar results are obtained using capacitance spectroscopy in a MOS-like structure with the nc-Si SL. In addition, we observed photocurrent oscillations with a frequency of several kHz. Our explanation is based on a carrier resonant tunneling in the nc-Si/SiO_2 SL.

11:30 AM T6.9
MULTI-MILLION ATOM MOLECULAR-DYNAMICS SIMULATIONS OF STRESSES IN Si(111)/a-Si_3N_4 NANOPIXELS. Martina E. Bachlechner, Andrey Omeltchenko, Phillip Walsh, Aiichiro Nakano, Rajiv K. Kalia, Priya Vashishta, Concurrent Computing Laboratory for Materials Simulation, Dept. of Physics & Astronomy, Dept. of Computer Science, Louisiana State University, Baton Rouge, LA; Ingvar Ebbsjò, University of Uppsala, SWEDEN; Anupam Madhukar, University of Southern California, Los Angeles, CA.

The interface structure and stress distribution in Si(111)/a-Si_3N_4 nanopixels are studied using molecular-dynamics simulations on parallel computers. Bulk Si is described by the Stillinger-Weber potential and Si_3N_4 is represented by a combination of two- and three-body interactions which include steric, charge transfer, polarizability and covalent forces. The charge transfer at the interface is extracted from self-consistent LCAO electronic structure calculations. The MD simulations for Si(111)/a-Si_3N_4 nanopixels involve three pixel sizes: 25nm, 50 nm, and 70 nm (the corresponding systems consist of 4 million, 10 million, and 27 million atoms, respectively). In all these systems we find stress domains at the interface which persist into the silicon substrate. The nature of the stress domains will be discussed. Supported by the Austrian Fonds zur Förderung der Wissenschaftlichen Forschung project no. J01444-PHY, the AFOSR, DOE, NSF, USC-LSU MURI from DARPA, ARO, and LEQSF.

11:45 AM T6.10
NON-VOLATILE MEMORY EFFECTS OF ION-BEAM SYNTHESIZED Ge AND Si NANOCLUSTERS IN THIN SiO_2 - LAYERS: ELECTRICAL CHARACTERIZATION VS. MICROSTRUCTURE. Thoralf Gebel, Johannes von Borany, Wolfgang Skorupa, Wolfhard Moeller, Forschungszentrum Rossendorf, Institute of Ion Beam Physics and Materials Research, Dresden, GERMANY; Karl-Heinz Stegemann, Hans-Juergen Thees, Mirko Wittmaack, ZMD GmbH, Dresden, GERMANY.

Thin SiO_2 films of 20 and 30 nm thickness have been implanted with Ge^+ (12 .. 20 keV) and Si^+ (6 ..12 keV) ions to doses of 1 .. 7 x10^{15} cm^{-2}. After RTA at 950°C for 30 s under a Nitrogen atmosphere a poly-Si layer (300 nm) was deposited by LPCVD. Subsequently the poly-Si layer was doped with P^+ ions and several thermal treatment steps were carried out. Charge storage effects of the MOS capacitors have been studied trough I-V and high frequency C-V measurements. Positive voltage pulses lead to a positive flatband voltage shift of the C-V curve. Detrapping by applying negative voltage pulses leads to a negative shift. The achieved programming window for Ge based structures (2.0 V for 6V pulses) is higher than that for Si (0.18 V for 6 V pulses). However the retention times for Si based memories are longer. Microstructural investigations (RBS, XTEM) for Ge clusters showed two bands of clusters, one near the interface SiO_2/Si and one volume band. Derived from microstructural results the charge is supposed to be stored not only in the clusters but also in traps at the interface cluster / oxide or even in-between the clusters at mo-lecular centers, e.g. the neutral oxygen vacancy.